Samtec combines Advanced IC Packaging and Ultra Micro Interposer technologies to achieve optimized interconnect paths - from the bare die to an interface 100 meters away, and all insertion points in between - with expertise in:

- Package and substrate design
- System modeling and prototyping
- Assembly and electrical testing of finished goods
- Ultra low profile, high density and dual compression contact micro interposers
- Advanced IC packaging, including die attach, wirebond, flip chip, dam and encapsulation, and micro optics

Samtec offers end-to-end signal integrity support including full channel analysis, high data rate simulations, break out routing and application assistance.

Visit SamtecMicroelectronics.com or contact the Microelectronics Group at SME@samtec.com.

**Advanced IC Packaging**

- **Flip Chip and Underfill**
- **Precision Die Attach**
- **Fine Pitch Wirebond**
- **Dam and Encapsulation**

**Micro Interposers**

- **Ultra Low Profile**
- **Termination Flexibility**
- **Ultra High Density**
- **Profile and Pitch Flexibility**
MICRO INTERPOSPERS

END-TO-END SYSTEM DESIGN + CAPABILITIES

Samtec’s Z-Ray™ micro array interposers are ultra low profile, ultra high density, and highly customizable solutions ideal for complex IC-to-Board applications.

- Ultra low profile, high density arrays, with BeCu micro-formed contacts on 0.80 mm and 1.00 mm pitches
- Ultra flexible, with a variety of standard and custom configurations, including dual compression, solder ball, and an array of sizes and shapes
- Assembled into rugged low profile FR4 substrate under high pressure and temperature
- Choice of fastener options, including application specific designs, screw downs, quick install (easy on/off) and thermal spreaders

Contact zray@samtec.com for more information.

<table>
<thead>
<tr>
<th>STANDARD &amp; CUSTOM Z-RAY™ MICRO INTERPOSER CAPABILITIES</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Series</strong></td>
</tr>
<tr>
<td>Pitch</td>
</tr>
<tr>
<td>Stack Height</td>
</tr>
<tr>
<td>Total I/Os</td>
</tr>
<tr>
<td>Ruggedizing</td>
</tr>
<tr>
<td>Construction</td>
</tr>
<tr>
<td>Terminations</td>
</tr>
</tbody>
</table>

Z-Ray™ Ultra Low Profile Interposers

ULTRA HIGH DENSITY
Choice of 0.80 or 1.00 mm pitch grid
ZA8 Series for up to 1,200 contacts / in²
ZA1 Series for up to 1,024 contacts / in³

ULTRA LOW PROFILE
One piece design
Low profile 1.00 mm body height
Low 25 g of normal force with .008” (0.20 mm) contact deflection

ULTRA FLEXIBLE
Customer-specific stack heights, pin counts, pitches, shapes and plating thicknesses
Alignment and fastener options
Customizable in X-Y-Z axes
Quick-turn customizations with minimal NRE and tooling charges

Also Available & In Development

ULTRA HIGH DENSITY
Z-Ray™ on 0.635 mm pitch and 1000+ I/Os in development

MULTI-LAYER SYSTEM
Pitch spreaders and other embedded interconnect circuitry

MICRO COAX CABLES
34 AWG micro twinax cable on 0.80 mm pitch, 8 and 16 pairs standard
1.00 mm pitch with up to 1,024 contacts per square inch

0.80 mm pitch with up to 1,200 contacts per square inch

Ultra low profile 1.00 mm body height

Fastener options

Dual compression contact system Single compression with solder balls

MODULARIZATION WITH Z-RAY™

save PCB real estate • reduce cost • eliminate reworks & scrap • gain design flexibility
Samtec Microelectronics Group is positioned to provide you with complete signal chain support - from custom package and substrate design, to connector and cable selection, through signal integrity testing and debug of your full system - helping you ensure an optimized signal path.

- Advanced IC package and substrate design
- Flip chip, die attach, wirebond, dam, encapsulation and lid attach
- Modeling and prototyping
- Testing and debug
- In-house optical engine design, manufacturing and packaging

Samtec’s worldwide Signal Integrity Group is dedicated to helping you determine and implement the most streamlined signal path possible, with support including full channel analysis, high data rate simulation, break out region design and routing, interconnect selection and application assistance.

Visit SamtecMicroelectronics.com for more information, or contact the Microelectronics or Signal Integrity Groups directly at SME@samtec.com or SIG@samtec.com.

Complex Package Assembly

FLIP CHIP & UNDERFILL

PRECISION DIE ATTACH

FINE PITCH & LOW PROFILE WIREBOND

DAM, ENCAPSULATION & LID ATTACH
LEADING-EDGE TECHNOLOGIES + CONTINUOUS INNOVATION

Samtec Microelectronics Group is positioned to support many industry-specific IC packaging applications. We provide leading-edge technologies and on-going development to ensure we are on the forefront of advanced IC packaging design and manufacturing.

Our manufacturing facility in Colorado Springs, Colorado, supports all areas of advanced IC packaging design, assembly, testing and manufacturing. Our technologies are supported by a reliable and accessible manufacturing infrastructure, along with full in-house signal integrity and system support.

Samtec adheres to a number of industry standard certifications and practices, including:
- TS 16949
- ISO 9001
- Environmental Compliance (RoHS)
- MIL-STD-883
- ITAR Regulation Compliance

Visit SamtecMicroelectronics.com for more information, or contact the Microelectronics or Signal Integrity Groups directly at SME@samtec.com or SIG@samtec.com.

MEDICAL & HEALTHCARE

Technologies / Capabilities
- MEMs
- Image packaging
- Custom IC package design
- Stacked and custom die
- Chip-scale interconnects

End Products
- Neuromodulation
- Implantable pressure sensors
- Surgical assistance robotics
- Endoscopes
- Ultrasound
- DNA and blood analyzers
- Control devices
- Ventilators
- Implantable devices
- Diagnostic meters
- Patient monitoring
- Heart rate and fitness monitoring
- Optical 3D surface scanners
- ECG, portable ECG and EEG
AVIONICS & DEFENSE

Technologies / Capabilities
- Compliant to MIL-STD-883
- ITAR Compliant
- Tin-only and Tin-Lead
- Custom design and assembly

End Products
- PAA (Phased Array Antenna)
- Missile control
- Data converters
- Avionic pressure sensors
- Hermetic package assemblies
- Laser modules
- Digital signal processors
- Microcontrollers
- Power management
- Analog to digital converters
- FIFOs
- Autonomous vehicle modules

OIL, INDUSTRIAL & COMMERCIAL

Technologies / Capabilities
- Micro footprint
- Flip chip, MEMs, BGA
- Thermal management
- Custom design and assembly
- Optics packaging

End Products
- Geophone seismic sensors
- Downhole sensor assemblies
- Communications
- Automotive
- Optical assemblies
- Smart grid and energy
- Test and measurement
- Digital storage
- Automation
- Motor drive and control
- Servers
DESIGN RULES & GUIDELINES

ADVANCED DESIGN + ASSEMBLY CAPABILITIES

Samtec Microelectronics Group has an extensive offering of advanced package design and assembly capabilities as well as the ability to assist in choosing the best technology and materials for your specific application.

In addition to substrate and package design, flip chip, die attach, wirebond and sealing, our capabilities also include thermal management, wafer dicing, lid attach and marking.

The following dimensions are designed to help release product to manufacturing as quickly as possible. Please contact Samtec Microelectronics Group at SME@samtec.com if you have tighter requirements.

Flip Chip

Basic guidelines for laying out flip chip substrates including pad design rules, package sizes, solder ball specs, flux, pad pitch and layout, and general structure:

PACKAGE SIZE
Smallest size (approx.): 10 mm x 10 mm
Largest size (approx.): 63 mm x 63 mm

SOLDER BALL MATERIAL TYPE
Eutectic Pb:Sn = 37:63
Pb-Free

SUBSTRATE BGA SOLDER BALL SIZE
Smallest (approx.): 0.018" diameter
Largest (approx.): 0.025" diameter

FLUX
TacFlux−025 & WS−609
Other no-clean flux-types, water soluble flux-types

SUBSTRATE BGA PAD PITCH
Closest pitch (approx.): 0.80 mm x 0.80 mm
Furthest pitch: no constraint
Any configuration of the pad layout is acceptable

TYPICAL SUBSTRATE STRUCTURE

LAYER THICKNESS (TYPICAL)

<table>
<thead>
<tr>
<th>Location</th>
<th>Standard (µm)</th>
<th>Custom (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Substrate</td>
<td>800</td>
<td>400*</td>
</tr>
<tr>
<td>Core Cu</td>
<td>25</td>
<td>21</td>
</tr>
<tr>
<td>Build Up Cu</td>
<td>14.5</td>
<td>2</td>
</tr>
<tr>
<td>Insulation Layer</td>
<td>33</td>
<td>12</td>
</tr>
<tr>
<td>Solder Resist Layer</td>
<td>21</td>
<td>18</td>
</tr>
<tr>
<td>Nickel Plating</td>
<td>3 – 7</td>
<td></td>
</tr>
<tr>
<td>Gold Plating</td>
<td>0.03 – 0.12</td>
<td></td>
</tr>
</tbody>
</table>

No. of Build Up Layers: 1, 2, 3, 4 per side; No. of Core Layers: 2, 4
*Coreless also available

SPECIFICATIONS (TYPICAL)

<table>
<thead>
<tr>
<th>Item</th>
<th>Standard (µm)</th>
<th>Custom (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A  Flip Chip Pad Dia. (Solder Resist Opening)</td>
<td>100</td>
<td>75</td>
</tr>
<tr>
<td>B  Flip Chip Pad Metal Land Diameter</td>
<td>145</td>
<td>100</td>
</tr>
<tr>
<td>C  Flip Chip Pad Pitch</td>
<td>225</td>
<td>130</td>
</tr>
<tr>
<td>D  Solder Bump Height</td>
<td>32 +/- 5</td>
<td></td>
</tr>
</tbody>
</table>
Die Attach

- Minimum distance between surrounding square of fiducial and neighboring objects must be 0.048 mm
- Gray level contrast between background and fiducial must be a minimum of 100 gray levels out of 256
- Background of fiducial must not have a structure & background must be single-colored gray level
- Maximum die size for dipping: 50 mm x 50 mm
- No waffle-pack handling for die < 1 mm^2
- Maximum length to width ratio for components: 5:1
- Saw kerfs must be at least 25μm and into the dicing tape (through the entire wafer thickness)
- Die attach materials can be non-conductive, conductive, die-attach-films (DAF) and solder preforms; other processes can be discussed per customer requirements

Wirebond

Plating and layout requirements for substrate pad design as well as wire parameters:
- Wedge Bond: ENIG plating is acceptable; typical wire types are Al, Au and Pt
- Ball Bond: ENEPIG plating is recommended; typical wire types are Au and Cu

Processes that use Au ball bond, require Gold plate per MIL-G–45204, Type III, Grade A, Class 1:
- 99.9% purity minimum
- < 90 Knoop hardness
- 50μ" thick, minimum

Dam & Encapsulation

- Maximum encapsulation thickness (board surface to top of encapsulation): 0.024" (600)
- Automated dispense tool heated work area: 12" x 16"
- Total work area: 20" x 30"
- Machine positioning accuracy and repeatability: +/- 0.001"

---

### TOP DOWN

- **A Overlap of Die Attach Ground Plane to Die Edge**
  - Organic (min) Fishing (µm): 0.020 (500)
  - Ceramic (min) Fishing (µm): 0.020 (500)

- **B Space Between Die Attach Ground Plane to Wirebond Pad**
  - Organic (min) Fishing (µm): 0.020 (500)
  - Ceramic (min) Fishing (µm): 0.020 (500)

- **C Space Between Fiducial Edge to Die Attach Ground Plane Edge**
  - Organic (min) Fishing (µm): 0.010 (250)
  - Ceramic (min) Fishing (µm): 0.006 (150)

### DIE ATTACH REQUIREMENTS

<table>
<thead>
<tr>
<th>Description</th>
<th>Organic (min) Fishing (µm)</th>
<th>Ceramic (min) Fishing (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Die Size</td>
<td>0.010* (250)</td>
<td>0.010* (250)</td>
</tr>
<tr>
<td>A Overlap of Die Attach Ground Plane to Die Edge</td>
<td>0.020* (500)</td>
<td>0.020* (500)</td>
</tr>
<tr>
<td>B Space Between Die Attach Ground Plane to Wirebond Pad</td>
<td>0.020* (500)</td>
<td>0.020* (500)</td>
</tr>
<tr>
<td>C Space Between Fiducial Edge to Die Attach Ground Plane Edge</td>
<td>0.010* (250)</td>
<td>0.006* (150)</td>
</tr>
</tbody>
</table>

### PACKAGE ENCAPSULATION RULES

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
<th>Organic (min) Fishing (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Dam Width</td>
<td>0.012&quot; (300)</td>
</tr>
<tr>
<td>B</td>
<td>Space of Dam to Wirebond Lead Edge</td>
<td>0.012&quot; (300)</td>
</tr>
<tr>
<td>C</td>
<td>Space of Fiducial to Dam*</td>
<td>0.007&quot; (175)</td>
</tr>
<tr>
<td>D</td>
<td>Overlap of Encapsulation to Top of Wirebond Loop</td>
<td>0.007&quot; (175)</td>
</tr>
<tr>
<td>E</td>
<td>Height of Encapsulation**</td>
<td>= A / 2</td>
</tr>
</tbody>
</table>

*Must be outside encapsulated region
**Board surface to top of encapsulation