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Using Full Wave Solvers for Practical Analysis of Capacitor Mounting Structures

Scott McMorrow, Teraspeed Consulting Group LLC
scott@teraspeed.com

Fabrizio Zanella, CST of America
fabrizio.zanella@cst.com

Steve Weir, Teraspeed Consulting Group LLC / IPBLOX
steve@teraspeed.com

Abstract

High frequency ceramic capacitors used for power distribution system (PDS) bypass and serial data link DC blocking applications are limited in performance by their series inductance and parasitic capacitance when mounted on a PCB. Inductance ultimately limits the performance of a capacitor in bypass applications, whereas parasitic capacitance and inductance limits performance in DC blocking applications. Accurate modeling of capacitors and their mounting structures is a critical link during the design and modeling of PDS and serial data links, yet rarely is this done, instead relying upon manufacturer supplied information or guesswork.

Land patterns and via positions on bypass capacitors have a major impact on device performance, however, these are influenced in some part by the physical capacitor geometry and construction. It is difficult to accurately model these effects with conventional techniques, and time consuming to perform accurate structure measurements. However, 3D full wave simulators are capable of performing just such modeling quickly and accurately. In this paper we will show techniques for the modeling of bypass capacitors, along with accurate S-parameter extractions, which can be used for the purpose of further PDS full-wave S-parameter evaluations, and some comparisons to measured data.

Authors Biography

S. McMorrow is an experienced technologist with over 20 years of broad background in complex system design, interconnect & Signal Integrity engineering, modeling & measurement methodology, engineering team building and professional training. Mr. McMorrow has a consistent history of delivering and managing technical consultation that enables clients to manufacture systems with state-of-the-art performance, enhanced design margins, lower cost, and reduced risk. Mr. McMorrow is an expert in high-performance design and signal integrity engineering, and has been a consultant and trainer to engineering organizations world-wide.

F. Zanella has over 15 years of experience working on Signal Integrity characterization of high speed digital systems. Mr. Zanella has worked for several companies, including Teradyne and EMC Corporation. At these companies Mr. Zanella led the signal integrity efforts to improve the high speed performance of system level, pc board and component designs. Currently he is a support manager at CST of America, a worldwide provider of full wave electromagnetic software. In his role he leads the application engineering team in North America; tasks include providing pre and post sales support to customers, conducting training classes and writing technical papers.

S. Weir has more than 20 years of industry experience and holds 17 U.S. patents. He has architected a number of packet and TDM switching products. Mr. Weir is a recognized expert in power delivery and a frequent contributor to the SI-list signal-integrity reflector.

Introduction

Several things should be considered when designing a power distribution system (PDS) utilizing multi-layer ceramic chip (MLCC) capacitors. Among these are the inductance of the mounted capacitor, the package inductance, the plane spreading inductance and number of capacitor vias. The plane spreading inductance limits the effectiveness of the capacitor. With higher performance bypass capacitors, several vias are used to provide multiple connections to the ground or VDD planes. These vias cause perforations in the planes, which degrades the signal return path and results in increased plane spreading impedance.

The position of high performance bypass capacitors is critical, and is most sensitive on the layers closest to the IC. New capacitor design technologies are available, such as X2Y capacitors. These capacitors consist of a 6 via pattern which results in a 4 terminal device; this design provides a significant improvement in the control of the return path, and subsequent reduction in total loop inductance.

The simulations of the various bypass capacitor effects on the quality of the PDS are performed with a commercially available 3D full wave simulator. Multilayer capacitors are simulated, and the 3D full wave tool provides Touchstone files or HSPICE models which can be used in circuit simulators.

Both Time Domain and Frequency Domain simulations are performed in order to verify the model results. Special test fixtures have been designed to accurately measure bypass capacitors of various sizes. The models are correlated against the measured data, and optimization analysis is then performed with the 3D full wave simulator to establish optimum settings for the capacitor land patterns and via positions.

Multi-layer Ceramic Chip Capacitor Basics

There have been significant advances recently in capacitor manufacturing. New ceramic material choices allow for increased capacitance values for small packages. Bypass capacitor values of 1 uF, 2.2 uF, and 4.7 uF in 0402 packages were not possible 3-4 years ago. Multilayer Ceramic Chip (MLCC) capacitors provide these higher capacitor values, and have improved inductance and impedance over 0603 package designs.

An MLCC capacitor (figure 1) consists of two sets of inter-leaved electrodes. Each electrode set is connected to one end of the MLCC assembly, and terminated with tin plated metallization. The capacitance value of an MLCC is:

$$C = \frac{(K)(n)(A)}{(d)}$$

C = capacitance value

K = dielectric constant

n = number of layers (n + 1 electrodes)

A = area of electrode overlap (figure 2)

d = dielectric thickness (between layers)

The larger capacitance values on MLCCs are achieved by using a larger dielectric constant, increasing the number of layers, increasing the electrode area, and using thinner dielectric layers. The design of MLCCs is cost effective; larger capacitance values are possible than conventional technology at lower prices. With this technology, doubling of capacitance values is achievable approximately every 2 years. MLCCs have lower Equivalent Series Resistance (ESR), lower Equivalent Series Inductance (ESL), lower Impedance (Z), and less temperature rise than conventional capacitors.

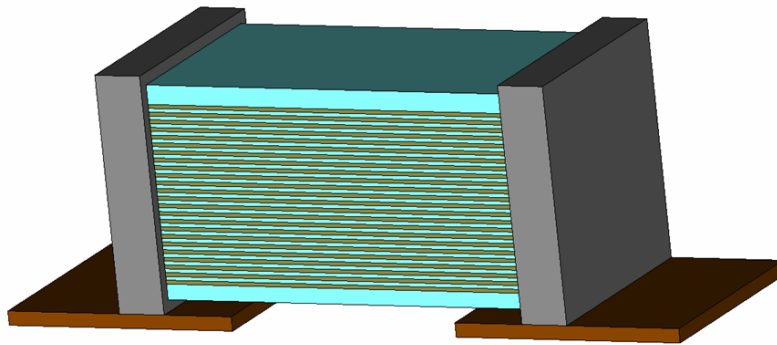
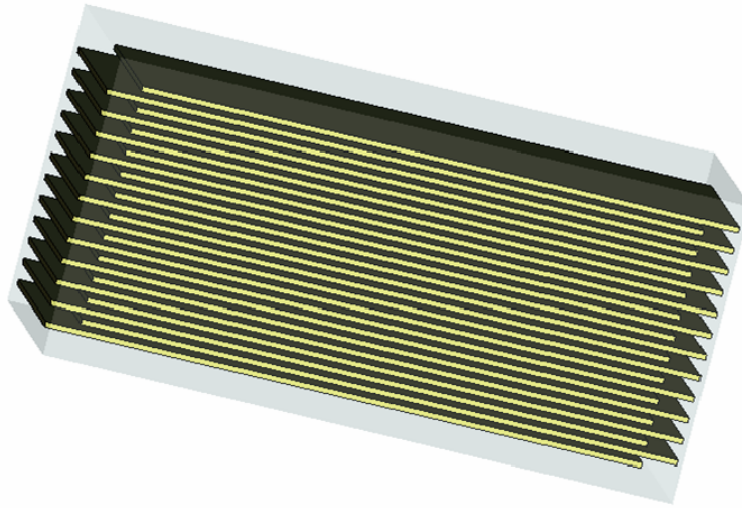


Figure 1 – Multi-layer ceramic capacitor with fully populated plates.



Material	Tin
Type	Lossy metal
Mue	1
El. cond.	8.7e+006 [S/m]

Figure 2 – MLCC electrodes showing plate overlap.

Over the past two decades, the volumetric efficiency (VE) of MLCC, in $\mu\text{F}/\text{cm}^3$, has increased by a factor of 10:1 every 4 to 5 years. From 1994 to 2005, VE for 0603 a packaged capacitor rose from 10 to 10,000 $\mu\text{F}/\text{cm}^3$, an increase of 1000:1. Increased VE has been accomplished through material science and advancement in manufacturing processes that have decreased the thickness of BaTiO₃ layers used in X5R and X7R applications, decreased the thickness of metal electrode layers, and have increased the total number of active layers. As a result, for 0603 class 2 MLCC devices, the maximum capacitance rose from 0.1 μF in 1997 to 10 μF at present day. Although this linear relationship is expected to taper off as the limits of the current materials and manufacturing processes are exhausted, 0602 devices with a maximum capacitance of 47 to 100 μF are definitely within the realm of possibilities by 2010.

Current PCB manufacturing is trending towards the use of smaller sized capacitors for space savings, along with an additional side benefit of reduced mounted inductance. As a result, development of higher VE MLCC devices seems to be focused on 0402 packaged components where 1, 2.2 and 4.7 μF devices are now currently available, with a VE approaching 50K $\mu\text{F}/\text{cm}^3$, and 0201 packages components where 0.1 and 0.22 μF devices, with a VE approaching 22K $\mu\text{F}/\text{cm}^3$. This has significant implications for the usage of MLCCs in high bandwidth power bypass applications.

MLCCs are built with a layered ceramic process. Alternate layers of ceramic material (X5R for example) and electrode material are applied in a low-cost, high volume ceramic process. For thermal/mechanical integrity, plates are symmetrically layered around the center line of the device, so that stresses are equalized, much like planes in a printed

circuit board. For manufacturing efficiency, plate and dielectric thickness are often identical for all capacitance values within a device family. Thus, only the maximum capacitance value for a given manufacturing process will have electrode plates that populate the entire body of the device. All other lower capacitance values will use less plates positioned around the center-line, effectively raising the height of the bottom plate with respect to the printed circuit board, (figure 3). *Since the loop inductance of a mounted capacitor in a bypass application is dependent upon the total loop area of the power/ground current path, the largest capacitor value in a given capacitor package size and manufacturing process will always have the lowest inductance.* All other lower values will have a higher inductance. As a result, irrespective of the remainder of the capacitor attach solution (pads, vias, and planes), it is physically impossible for there to be one value of inductance for all values of a given capacitor family!

Power delivery solutions, and associated simulation environments, which require the accurate knowledge and understanding of capacitor mounted inductance to formulate a robust non-resonant impedance profile, can be stymied by the lack of data published on variation in ESL with respect to the internal plate locations and capacitance of the device. In addition, as MLCC manufacturing techniques improve, with increased VE, system designs that were carefully simulated, designed, characterized and/or specified using a particular capacitance value, may find curiously that the inductance of specified capacitors tend to change during the course of manufacturing in the product life cycle. For 0402 package MLCC devices, ESL variations of up to 200 pH may not be unreasonable, based upon this study.

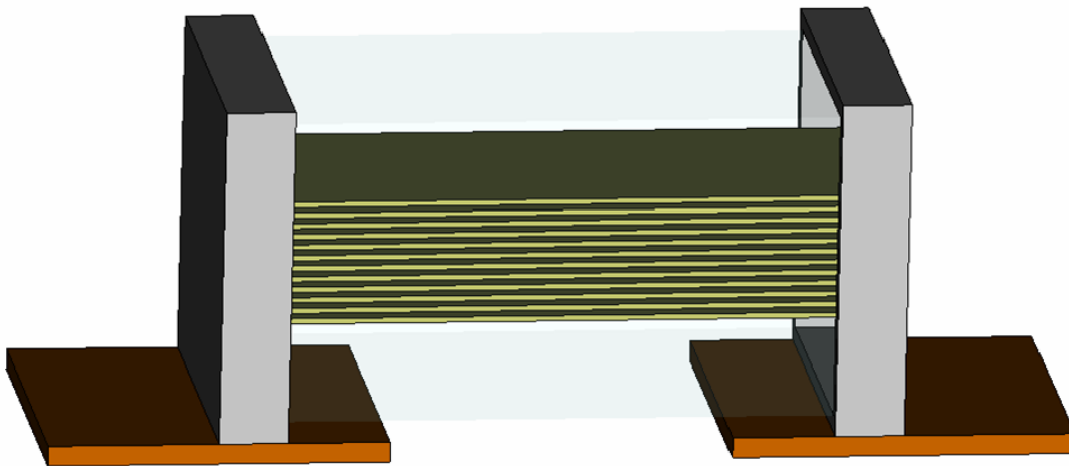


Figure 3 – MLCC with capacitance value lower than maximum.

3D Full-wave Modeling with Time and Frequency Domain Techniques

The commercial CST Studio Suite 2008™ software is used for the simulations of the capacitor landing patterns. The CST MICROWAVE STUDIO® tool (CST MWS), a full wave 3D EM modeler is part of the CST Studio Suite. CST MWS offers a choice of several solvers. For the simulations of the capacitor test fixture, the Transient and Frequency solvers were considered.

The CST MWS Time Domain or Transient solver uses the Finite Integration Technique (FIT). The meshing algorithm is hexahedral (HEX) and uses the following techniques: Perfect Boundary Approximation (PBA) and Thin Sheet Technique (TST). The Transient solver is very robust and can handle most applications. It's well suited for broadband, electrically large structures. Energy is injected into the structure and steps through time. All frequencies are included in one simulation, and the results are in time and frequency domain. Simulations are performed on a port-by-port basis. Typical 3D full wave models which are optimal for the Transient solver are: printed circuit boards, packages, connectors, antennas, waveguide components.

The CST MWS Frequency solver uses a tetrahedral (TET) mesh. Highly resonant, electrically small structures at narrow bands are optimal for the Frequency solver. A broadband frequency sweep is performed to achieve accurate S-parameters. This solver contains a very robust automatic mesh refinement and both an iterative and direct solver. Typical 3D full wave models for which the Frequency solver is optimal are: resonators, filters, structures with high Q, structures electrically small compared to the signal wavelength. Both the CST MWS Transient and Frequency solvers are used for the full wave simulations, in order to validate the results.

The CST MWS model of the capacitor test fixture (figure 4) materials used in the full wave simulation are:

FR4 substrate, dielectric constant = 4.25, loss tangent = .021

Copper plane under capacitor, test pads, vias

PEC (perfect electric conductor) test board planes

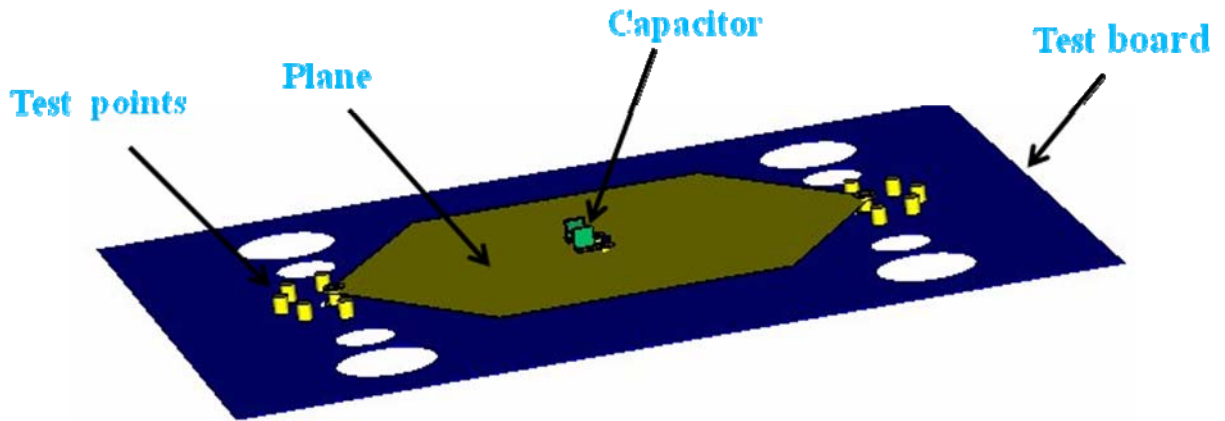


Figure 4 – Capacitor test fixture

The MLCC capacitor model, which resides in a 0402 package (figure 5) is constructed with the following materials:
BaTiO₃ ceramic, dielectric constant = 3300, loss tangent = .02
Nickel metal ends, tin plates, copper pads.

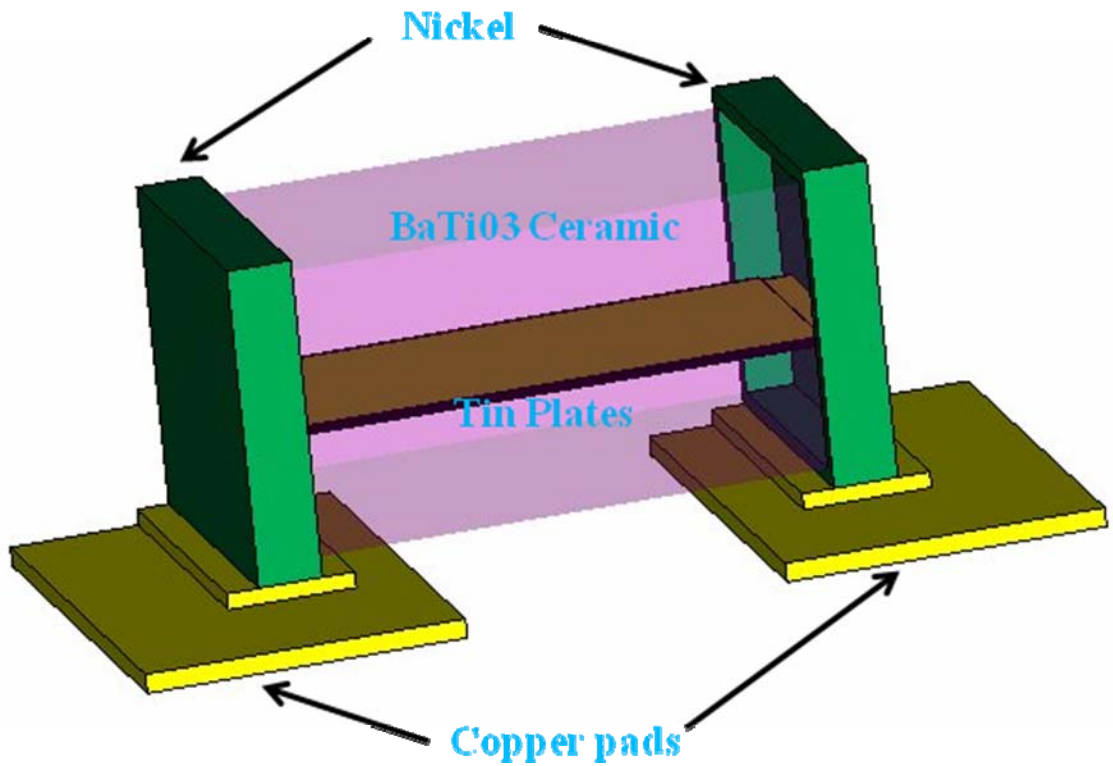


Figure 5 – MLCC capacitor model

The CST MWS simulation is performed using a tetrahedral mesh (figures 6, 7) for the Frequency solver and a Hexahedral mesh (figure 8) for the Transient solver.

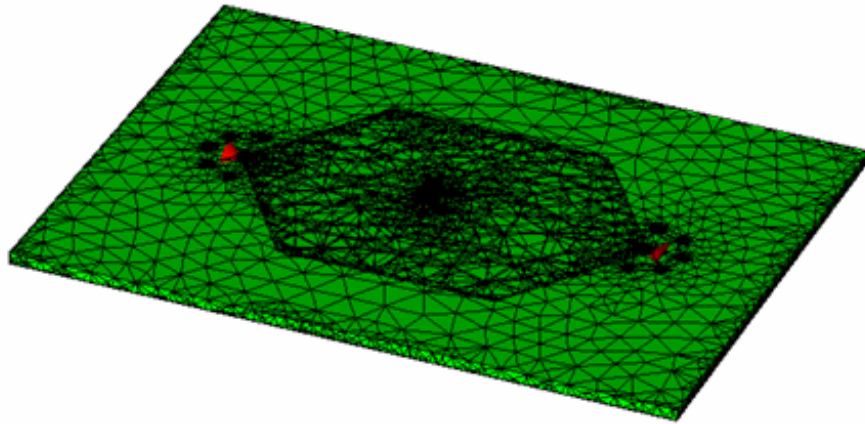


Figure 6 – Tetrahedral mesh of test fixture

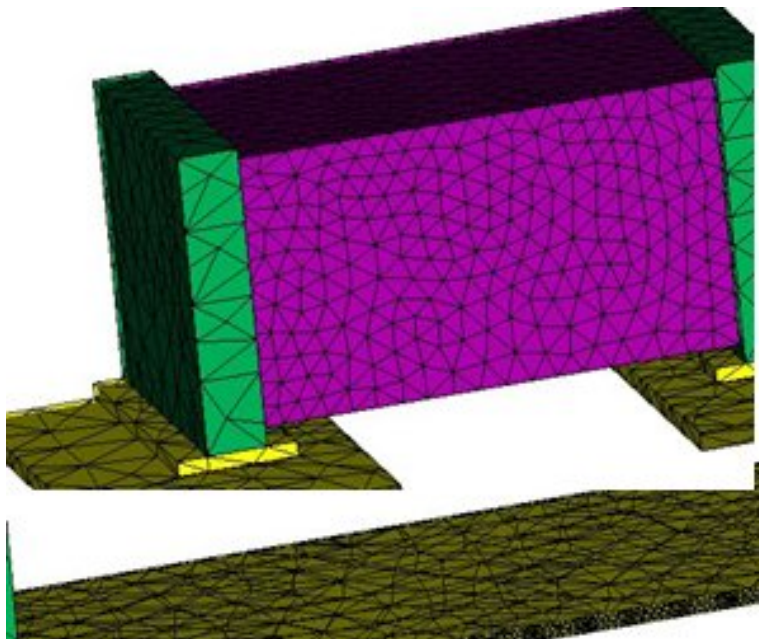


Figure 7 – Top, tetrahedral mesh of capacitor substrate, metal ends and pads. Bottom, detailed mesh of capacitor plates

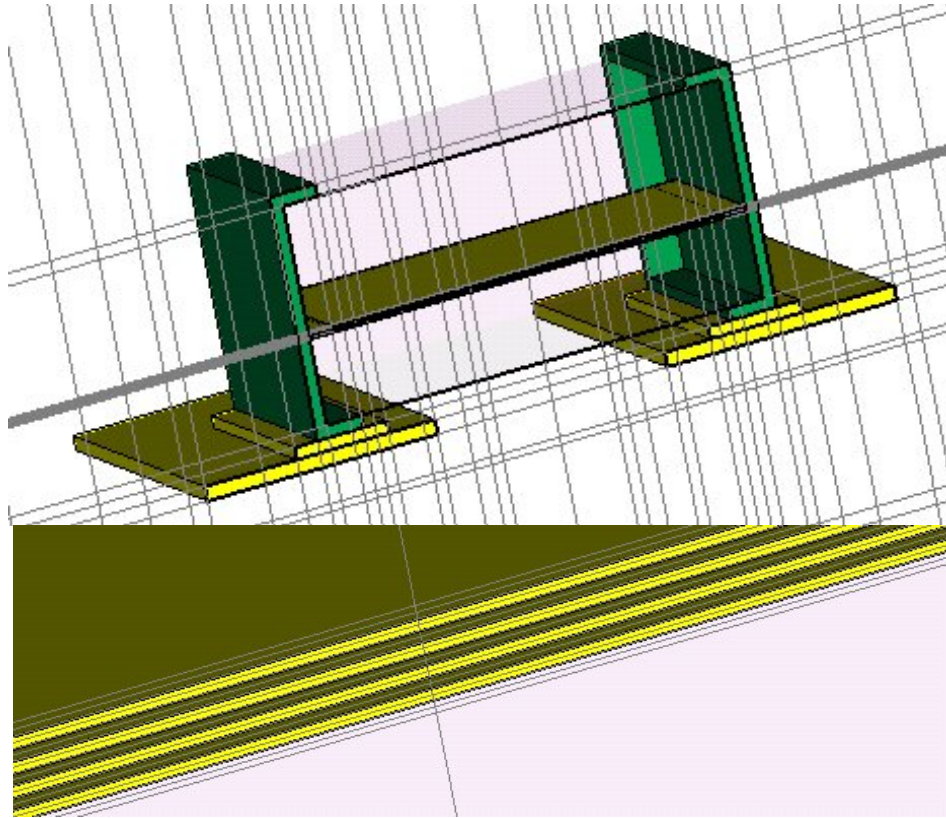


Figure 8 – Hexahedral mesh of capacitor (detail of plates on bottom).

The resultant S21 from the Frequency solver simulation is shown on Figure 9. The simulation is run at a frequency range of 0 to 10GHz. There is very close agreement between the Frequency and Transient solver simulations, as indicated in Figure 10.

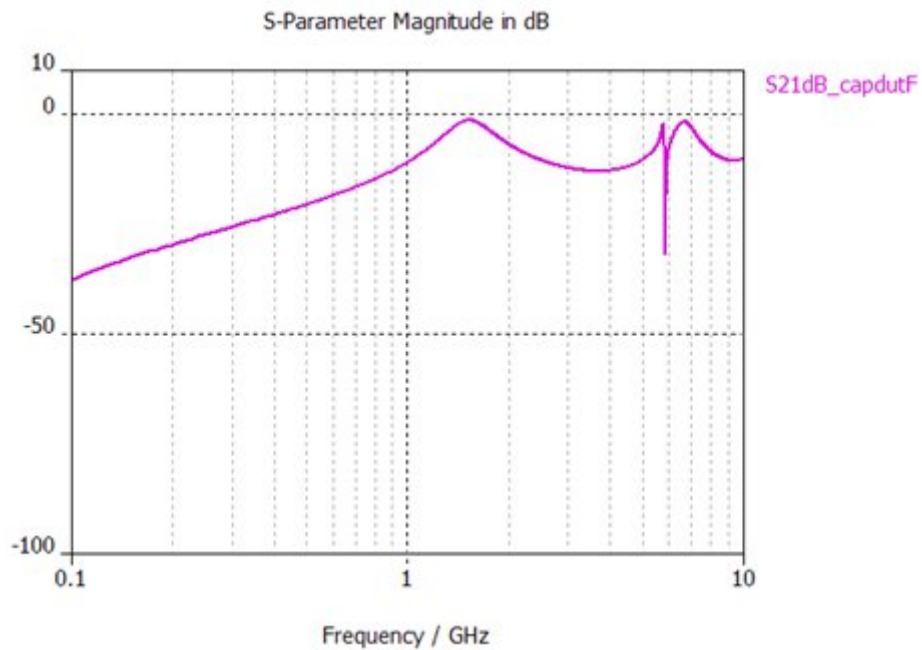


Figure 9 – Frequency solver S21(dB)

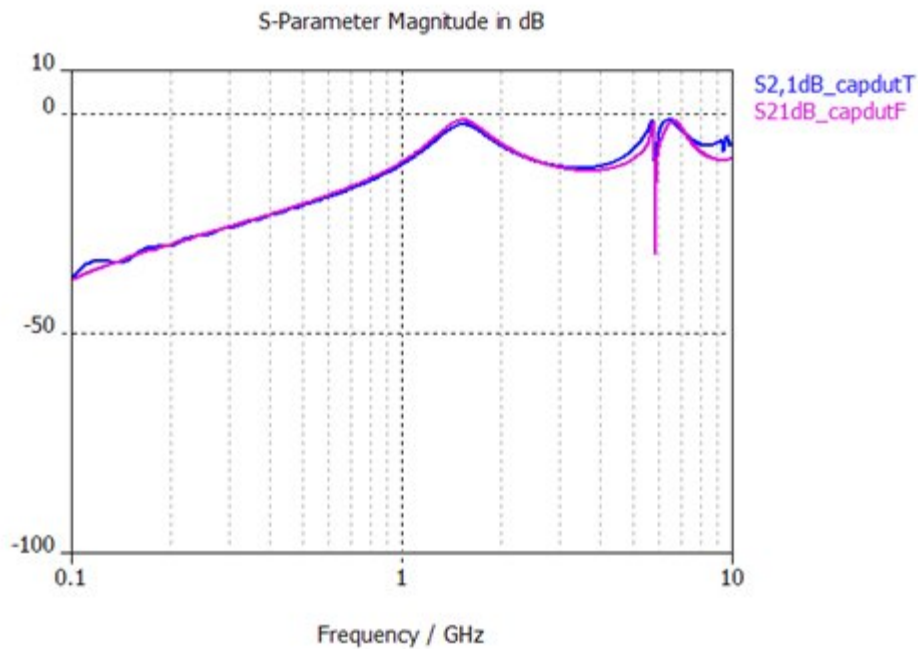


Figure 10 – Validation of Frequency and Transient solver S21(dB).

Modeling and Measurement Correlation of a MLCC Test Fixture

Transfer impedance measurements of a shunt capacitor bypass can be used to determine the impedance of capacitor shunt. The Norton equivalent of the VNA generator and receiver connected together is a 50 ohm source in parallel with a 50 ohm load, i.e. 25 ohms in parallel with the DUT shunt.

The voltage amplitude in dB is:

$$S21dB = 20 * \text{Log}_{10} * Z_{DUT} / (Z_{DUT} + 25)$$

The voltage amplitude is also:

$$S21(mag) = Z_{DUT} / (Z_{DUT} + 25)$$

Solving for Z_{DUT} :

$$Z_{DUT} = 25 * S21(mag) / (1 - S21(mag))$$

At any frequency other than the Series Resonant Frequency (SRF) of the capacitor, the impedance results from all three components, ESR, C, and ESL. Since:

$$Z_C = 1/j\omega C$$

$$Z_{ESL} = j\omega ESL$$

However, above the SRF and below the first parallel resonant frequency (PRF), impedance is dominated by inductance, since capacitive reactance decreases linearly with frequency, and inductive reactance increases linearly with frequency, while series resistance (ESR) remains relatively low for MLCC capacitors. As long as Z_C and Z_{ESR} are $\gg Z_{ESL}$, then the transfer impedance curve is in a linear ESL dominated region (figure 11), where the shunt inductance of the capacitor is:

$$Z_{ESL} = 2\pi f \times ESL$$

$$ESL = Z_{ESL} / 2\pi f$$

$$ESL = (25 * S21(\text{mag}) / (1 - S21(\text{mag}))) / 2\pi f$$

Where f = frequency.

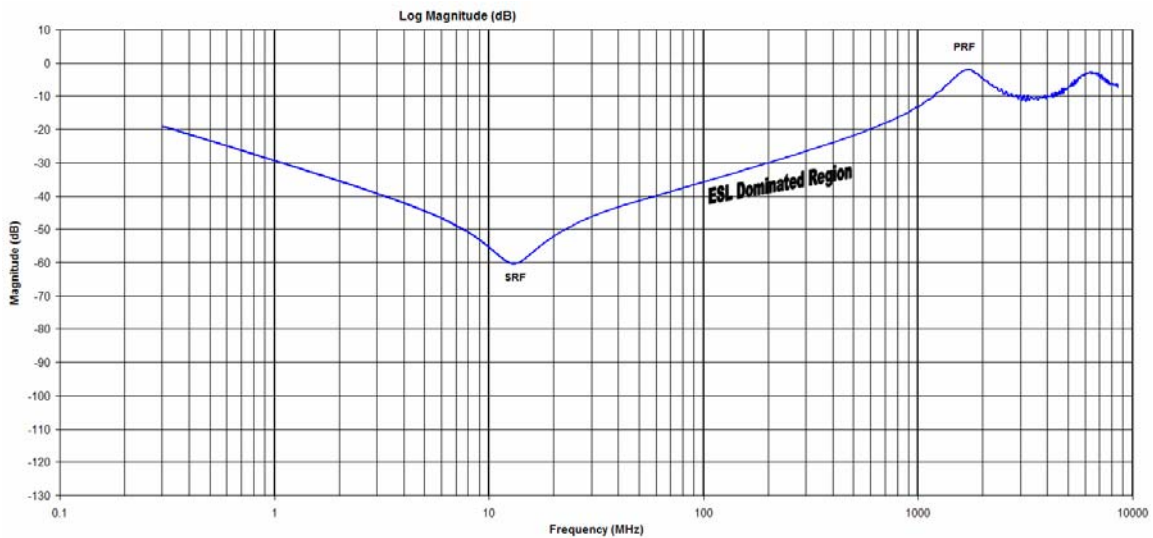


Figure 11 - 0.22 uF 0402 MLCC Capacitor Shunt Impedance Measurement.

Transfer impedance measurements were made of a 0.22 uF 0402 capacitor using the test fixture of figure 12, designed by Teraspeed Consulting Group LLC and Sigcon for high resolution capacitor inductance extraction.

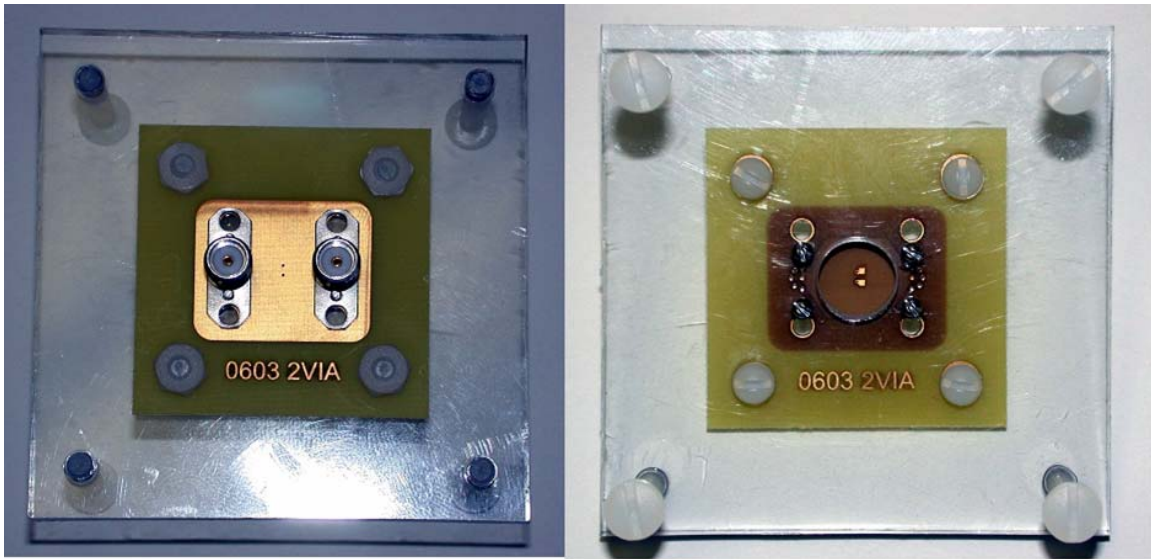


Figure 12 - 0.22 uF 0402 MLCC Capacitor Shunt Impedance Measurement.

Figure 13 shows a detailed view of the test fixture, where high bandwidth SMA launches are used to perform a transfer impedance measurement of a shunt DUT attached across a power and ground plane layer.

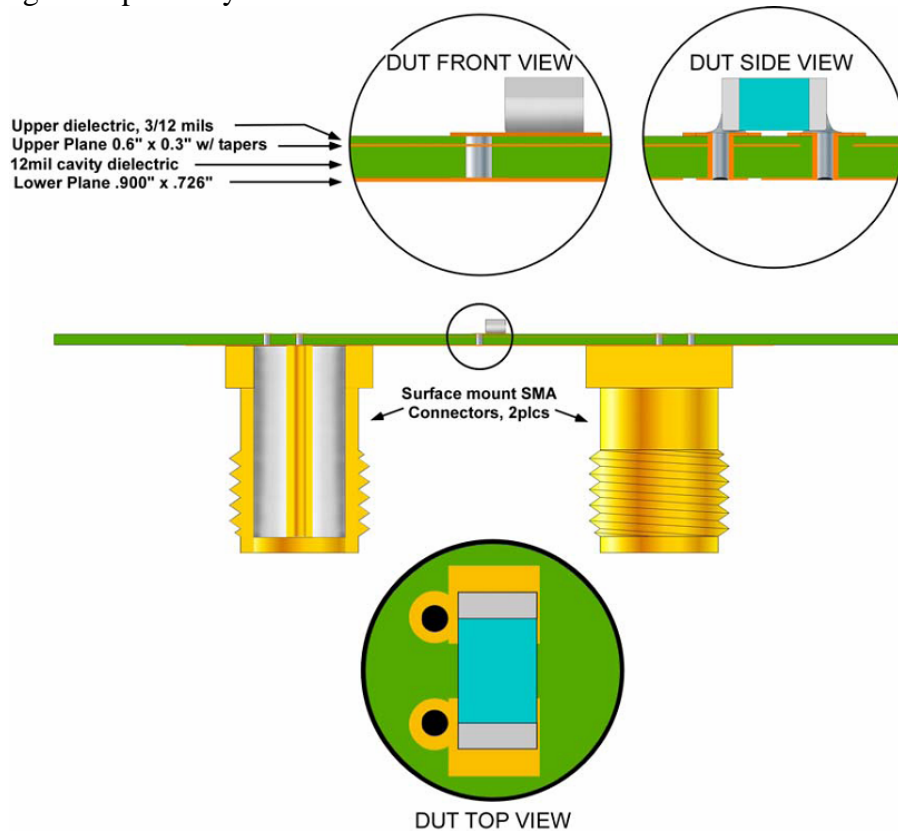
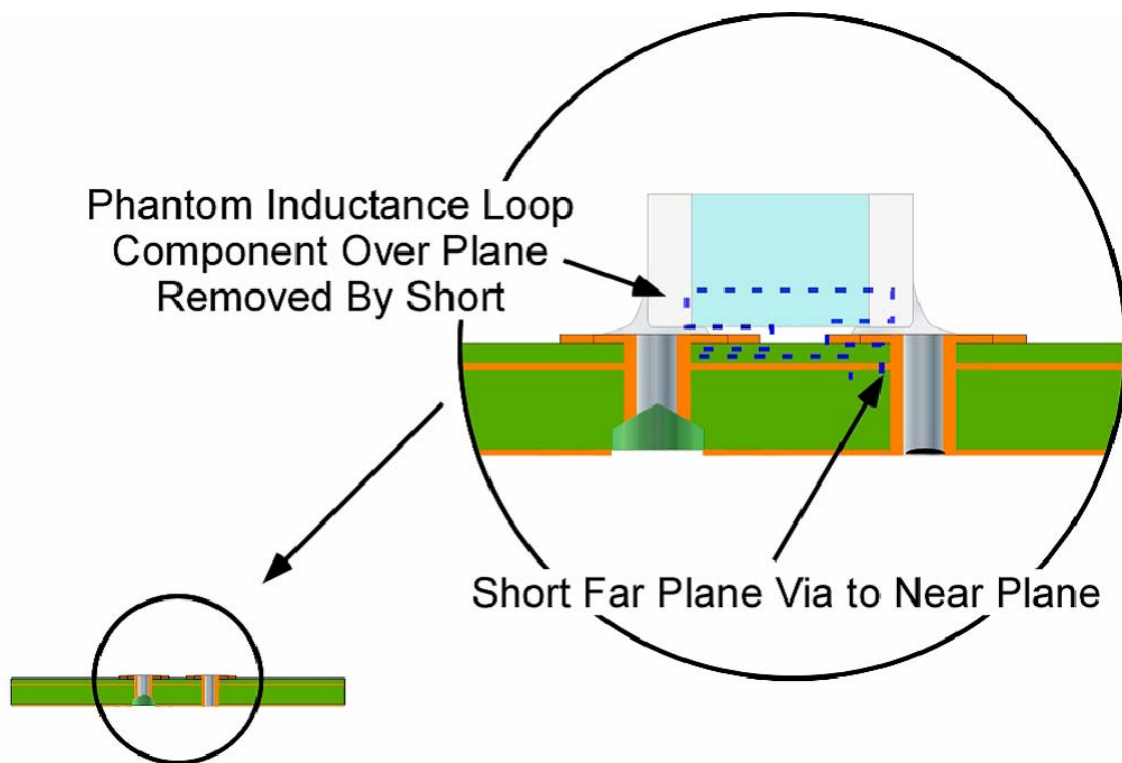


Figure 13 – Test Fixture Detailed View.

Two additional calibration structures are also provided. Figure 14 shows a diagram of the shorted via structure, where the mounting vias for the DUT are shorted between the power and ground planes. This structure removes the inductance of the DUT, pads and vias above the top plane and allows for a measurement of the inductance between the power and ground planes. An additional structure that is not shown, shorts the top layer DUT mounting pads, removing the inductance of the DUT from the measurement, which allows for a measurement of the total PCB mounting inductance.



Via short calibration

Figure 14 –Test Fixture Shorted Via Calibration.

The identical structures were modeled in CST Microwave Studio for full wave electromagnetic solutions, using the time and frequency domain solvers, as shown previously in figures 4-8, along with a model developed for the MLCC capacitor itself. Simulations were performed for three cases: Shorted Via, Shorted Pad, and DUT. In addition, several plate configurations of the DUT were modeled.

Using the transfer impedance measurements of figure 11 as a guide, we determined that the 100 to 500 MHz frequency range would be best for extraction of inductance, as this is

midway between the SRF and PRF frequencies of the mounted capacitor. Table 1 shows the results of the various measurement and simulation scenarios performed.

	100 MHz	200 MHz	300 MHz	400 MHz	500 MHz
Shorted Structures					
Via Short Time Domain Solver	107 pH	106 pH	107 pH	108 pH	109 pH
Via Short Frequency Domain Solver	113 pH	112 pH	113 pH	114 pH	115 pH
Via Short Measured	86 pH	85 pH	85 pH	86 pH	88 pH
Pad Short Time Domain Solver	379 pH	342 pH	367 pH	367 pH	374 pH
Pad Short Frequency Domain Solver	403 pH	404 pH	411 pH	423 pH	439 pH
Pad Short Measured	403 pH	404 pH	411 pH	421 pH	440 pH
2 mil MLCC DUT Cover Layer					
DUT Time Domain Solver	462 pH	485 pH	515 pH	532 pH	552 pH
DUT Frequency Domain Solver	506 pH	507 pH	518 pH	535 pH	709 pH
Actual DUT Measured	658 pH	646 pH	654 pH	672 pH	707 pH
8 mil MLCC DUT Cover Layer					
DUT Time Domain Solver	662 pH	640 pH	647 pH	671 pH	704 pH
Actual DUT Measured	658 pH	646 pH	654 pH	672 pH	707 pH

Table 1 – Test Fixture Inductance Extraction, Measured vs. Simulated.

Correlation to measured results is very good for both the time and frequency domain methods for the shorted pad structure. Time domain transfer impedance measurements are extremely sensitive to impedance mismatches that cause ringing in the transient response. Generally full wave transient simulations must be cut short before achieving a steady state response, which results in errors in the extracted s-parameters, whereas the frequency domain solver is sensitive to convergence error in trapezoidal meshing. Both approaches can achieve convergence to near-identical results, however care must be taken.

Correlation for the shorted via structure, shows some slight offset for both solvers. This can be reconciled if the actual measured structure has a slightly thinner dielectric layer thickness between the power and ground planes. Good correlation with the pad short method, indicate that the total PCB thickness for all layers is probably close to what was modeled, but that the outer layer is probably thicker, and the inner layers are probably slightly thinner.

Originally, correlation for the 0.22 uF 0402 MLCC capacitor was perplexing. As shown in the 2 mil MLCC DUT Cover Layer section of Table 1, both the time and frequency domain solvers show inductance values that are approximately 120 to 200 pH lower than what were measured across all frequency points. After further investigation, the authors determined that the discrepancy lay in the modeling of the capacitor electrodes.

Originally we had assumed that the device measured fully utilized all the body area of the capacitor with electrodes. This would require the bottom plate to reside at the minimum cover layer thickness of 2 mils. However, upon further research it turned out that the 0.22 uF Panasonic capacitor measured, part number ECJ-0EBOJ224K, was not the largest capacitance value in that technology family. Panasonic part number ECJ-0EBOJ105M is a 1.0 uF 6.3V X5R 0402 MLCC capacitor of the same family as the capacitor measured. As discussed previously, it is this capacitor that will fill the entire volume of the capacitor body, and have plates closest to the PCB. A .22 uF capacitor will fill only approximately 25% of the capacitor body, placing the lower most plate higher in the body. As a result, we chose to modify the capacitor model to place the lower plate, 8 mils above the bottom of the capacitor body, in the approximate position that it would be in the measured capacitor.

With the modified 8 mil MLCC DUT Cover Layer model, the time domain solver was able to produce extracted inductance values that are an extremely close match to the measured results. This potentially confirms our assumptions regarding the construction of this particular MLCC capacitor.

Summary

3D full wave simulators are capable of performing quick and accurate models of capacitor bypass structures. We have shown techniques for the modeling of bypass capacitors, along with accurate S-parameter extractions, which can be used for the purpose of further PDS full-wave S-parameter evaluations, and some comparisons to measured data. Further investigations are ongoing to determine the validity of some of our assumptions regarding the particular capacitors and PCBs measured in this study, and the modeling methods used.

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