Teraspeed Measurement Based IBIS Modeling Process

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Measurement Process Overview

- Collect data on component
- Develop a test plan
- Design a test fixture
- Measure the characteristics required
- Enter data into the system
- Build model
- Test model

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There is a lot of pre-work to do before we start to model a component. The most important is to determine how we are going to stimulate and measure the component.

All these steps must be completed before a completed model is produced.

Develop Test Plan

- From the data collected determine
  - Which pins to measure
  - Which techniques are required to stimulate the output(s)
    - JTAG
    - Test vectors
    - Etc.
  - Determine if a new test fixture is required

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The success of the rest of the process is dependent on getting the test plan in place. This drives the design of the test fixture. Determining which pins to measure and how we are going to measure them determines if we can build a model for any component.

Develop a Test Fixture

- Supply clean power to the device
- Access to pins that need to be driven
- Access to pins that need to be measured
- Any support circuitry required to operate the device

The test fixture allows us to power up the chip, control it and make the measurements required. The chip needs to get clean power. Signals that allow control of the outputs need to be available to our word generator. The signals we are going to measure need to be brought out to test points. Any additional circuitry required to get the chip to operate also has to be included on the test fixture.

Measurement Process

- VT data
  - 50 Ohms to ground and acquire rise and fall
  - 50 Ohms to Vcc and acquire rise and fall
  - Preserve timing relationships between waveforms

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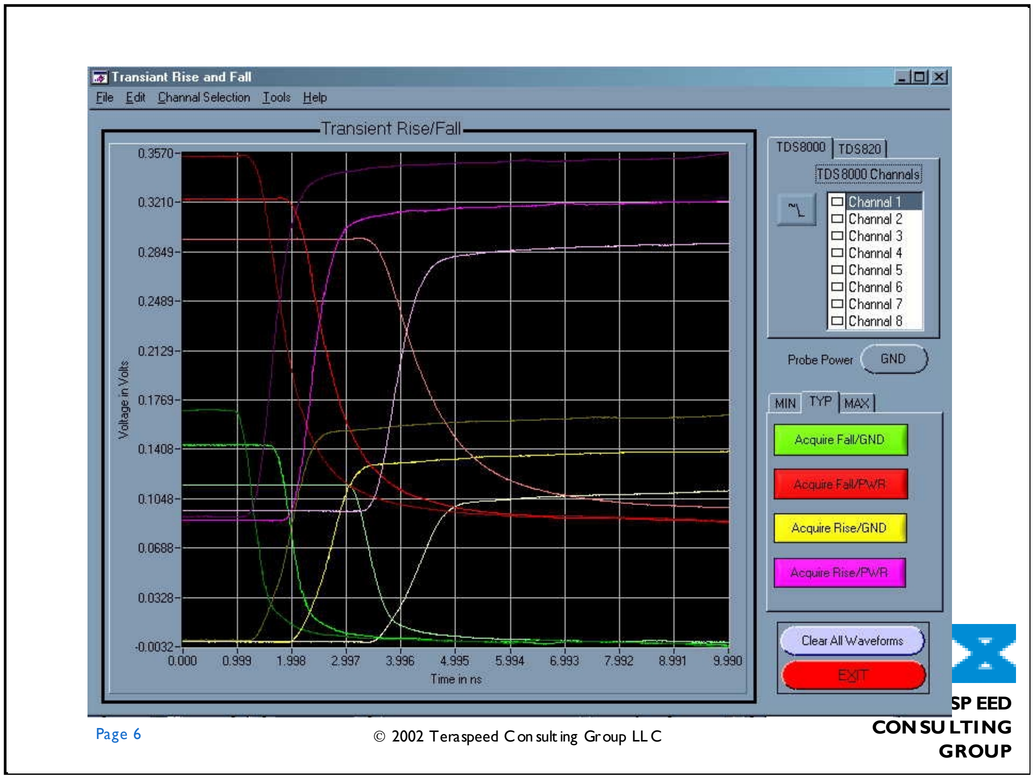
Taking accurate VT information is a key to making good IBIS models. The measurement system must have adequate bandwidth, at least 3 to 5 times the bandwidth of the signal of interest. For a part with a 100 psec risetime (3.5 GHz bandwidth) you need a scope of 10 to 15 GHz bandwidth.

IBIS is built around having the loads used in the model represent the actual load the driver will see in the final application. Most PCB runs lie between 40 and 65 Ohms. So the model should characterize the buffer at an equivalent level. 50 Ohms has been the standard load for IBIS models, a good compromise for the Zo of the traces on a typical board and the same as most T&M equipment is designed to work.

The four VT waveforms are acquired to show the turn-on and turn-off of the pull up and pull down devices. This is what happens when a driver drives a transmission line. When the driver transitions from low to high it has to charge the line starting with zero volts on the line. When it drives from hi to low it see a Zo tied to the high level and must ‘charge’ the line to the lower level. How the drive accomplishes this depends on how the pullup and pulldown devices turn on and off.

Keeping the time correlation between waveforms is very important. The scope must be triggered off some external event, not the waveforms of interest. This timing relations shows when one device turns on and the other turns off.



Here is a complete set of VT curves for a part measured over process, temperature and voltage. The upper set of waveforms are with the 50 Ohm termination tied to Vcc and the lower set for the output terminated to ground. It is easy to see the change in prop delay in the component from the max to typ to minimum set of conditions.

To make the measurements we need to get the buffer to toggle for the VT measurements and to into steady states (hi, low and off if appropriate) for the DC measurements.

To do this we try to make most components look like buffers, flip-flops, registers or stimulate them via the SCAN port using JTAG control. Some chips require complex setups such as SDRAM.

Measurement Process

- IV Data
  - Place output in high state
    - Sweep from 0 to Vcc + 1.2 Volts
  - Place output in low state
    - Sweep from –1.2V to Vcc
  - If appropriate get input or tri-state
    - Sweep from –1.2 to Vcc + 1.2 Volts

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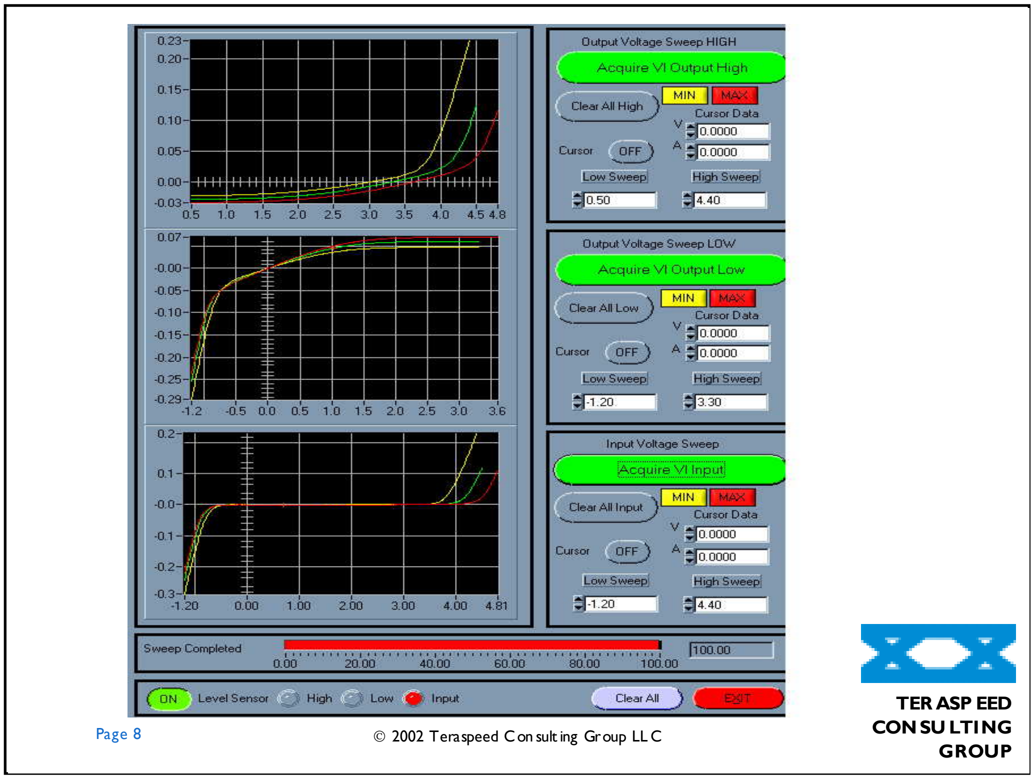
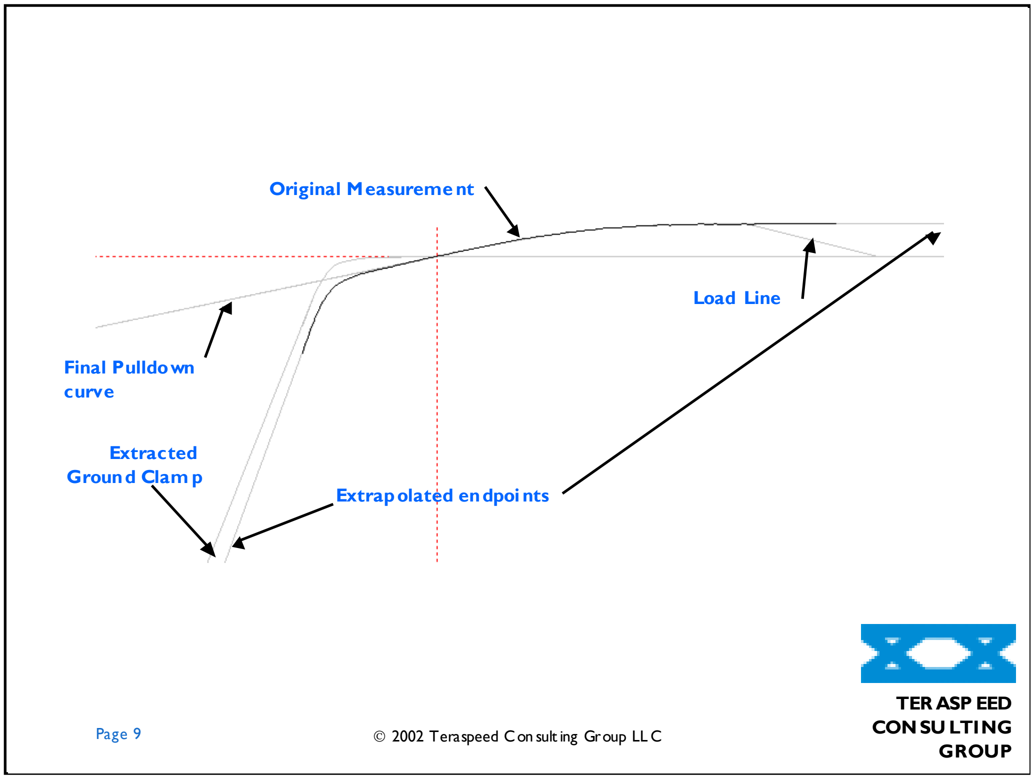
IBIS specifies buffers should be characterized over the –Vcc to 2Vcc range. This characterizes the buffer over the expected range of voltages it might see in an application. For example, if a driver were to send a rise to a receiver over a unterminated transmission line and the receiver had no powerclamp the voltage at the input of the receiver would be twice the incident waveforms amplitude. Since the line is unterminated the incident waveform would not be absorbed in a load and would have a positive reflection coefficient of 1, reflecting back twice the incident signal.

When making measurements we cannot expect the devices to be able to withstand such a wide range of voltages so we measure the characteristics over a limited range and extrapolate to the wider range. Teraspeed has found that measuring past the supply rails by 1.2 volts for most parts will protect the device and allow us to characterize the clamp structures if present. There are always exceptions to the rules. SiGe components are very sensitive and cannot be taken past the supply rails by more than about 0.4 Volts. Some devices will latch up by 0.8 Volts past the rail.



These are the IV characteristics of the same component over process, temperature and voltage. The upper window shows the pull up characteristics, the middle the pulldown and the lower the input.



•This shows the processing that goes on in one of our tools that extract the ground clamp from the pull down characteristic of a output only driver. First the original waveform is extended to the full IBIS –Vcc to 2xVcc range (not fully shown here). Then the pulldown characteristic is generated by extending the slope at ground of the resistive region of the curve to –Vcc. The new pulldown is then subtracted form the extended measurement curve to yield the extracted ground clamp curve.

•A similar process is used for the pullup curve/powerclamp.

Collect Component Data

- Pin data
  - Number
  - Signal
  - Package parasitics
  - Electrical specification
  - Timing test load
  - Diff pin pairs
  - Etc.

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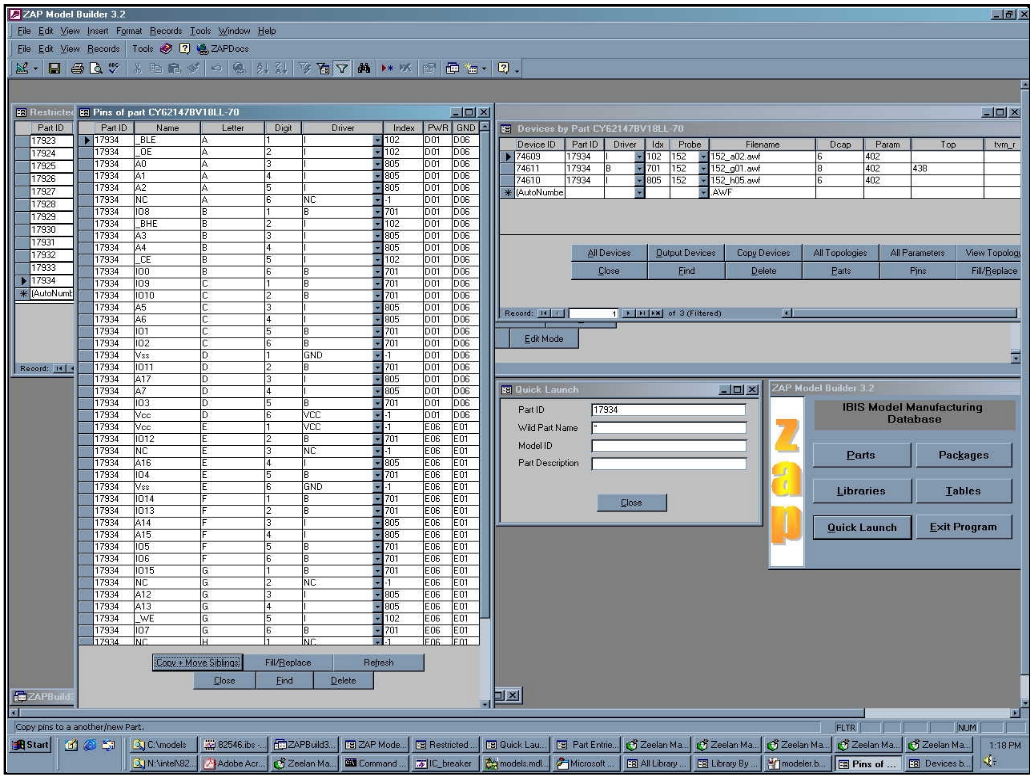
An IBIS file consists of three major parts. The header information, the pin information and the waveform data. We need to collect all the data about the component and use a database to store that information. The database stored the header and pin data. From the information above the pin section is produced. Most of this data is collected from the datasheet for the part. Package parasitics can be measured and stored in the database also.



This shows some of the screens in our database. All pin and specification data is stored in the database.

Build Model

- Build model
- Check with IBIS Golden Parser
- Load and check in a simulator

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Too may model makers neglect steps two and three in the process. There are too many models that will not pass the IBIS parser. Many models may pass the IBIS parser but do not have reasonable waveform in them.