

IBIS Present and Future

Bob Ross

(Past Chair, EIA IBIS Open Forum)

7th IEEE Workshop on
Signal Propagation on Interconnects
Hotel Garden, Siena, Italy
May 11-14, 2003



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IBIS and Outline

- **IBIS**
 - Input/Output **B**uffer **I**nformation **S**pecification
- IBIS History and Overview
- Algorithms
- Extensions
- Future
- Interconnects



References

- Web sites
 - <http://www.eigroup.org/ibis/ibis.htm> (IBIS home page)
 - <http://www.eda.org/pub/ibis/> (IBIS FTP site)
 - http://www.mentor.com/pcb/ibis_modeling.html
 - <http://www.teraspeed.com/>
 - <http://www.silicontech.com/home/seminar-index.shtml>
(Real Time video course by Arpad Muranyi, Intel)
- Books
 - Johnson, Graham, High-Speed Signal Propagation, 2003
 - Hall, Hall, McCall, High-Speed Digital System Design, 2000



Academic Contributions

- North Carolina State University
 - Spice to IBIS conversion utilities
- INSA, Toulouse, France
 - Integrated Circuits Electromagnetic Model (ICEM) development
- University of Missouri, Rolla
 - Pending EMC proposal based on consortium's research
- Several thesis projects
 - (France, Singapore, New York)
- Arizona State University
 - IBIS short course - Arpad Muranyi



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10 Year Anniversary

- Version 1.1 - June 1993 - August 1993
- Version 2.1 - June 1994 - December 1994
– ANSI/EIA-656
- Version 3.2 - June 1997 - April 2001
– ANSI/EIA-656-A and IEC62014-1
- Version 4.0 - July 2002 -
– More refinement and pending multi-lingual extension



Key Features for Commercial Use

- Electronically parsed table format
- Does not reveal proprietary process or architecture
- Developed from measurement or SPICE
- Suitable and compatible with PCB data bases (plugs in like a part)
 - Component centric vs. buffer centric SPICE
 - Automated rules based EDA analysis
- **Balances accuracy and model availability**



Elements of an IBIS Model

- Component Pinout
- Component Package*
- I/O buffers*
- Specification and information content
 - (e.g., thresholds, Model_type, timing test load)
- (Electrical Board Description (EBD) and future Interconnections)*
- * Also in SPICE models, but SPICE has availability, compatibility, speed issues

Industrial Support

- EIA IBIS Open Forum
 - 30+ members, 400+ on reflectors
 - Open, active meetings and summits
 - Free utilities (ibischk3, s2ibis2, etc.)
 - IBIS Quality Committee, IBIS User's Group
- EDA vendors
 - Nearly all EDA printed circuit board analysis tools
 - Many SPICE vendors (e.g., HSPICE B element)
- SI Reflector - 22% e-mail on IBIS



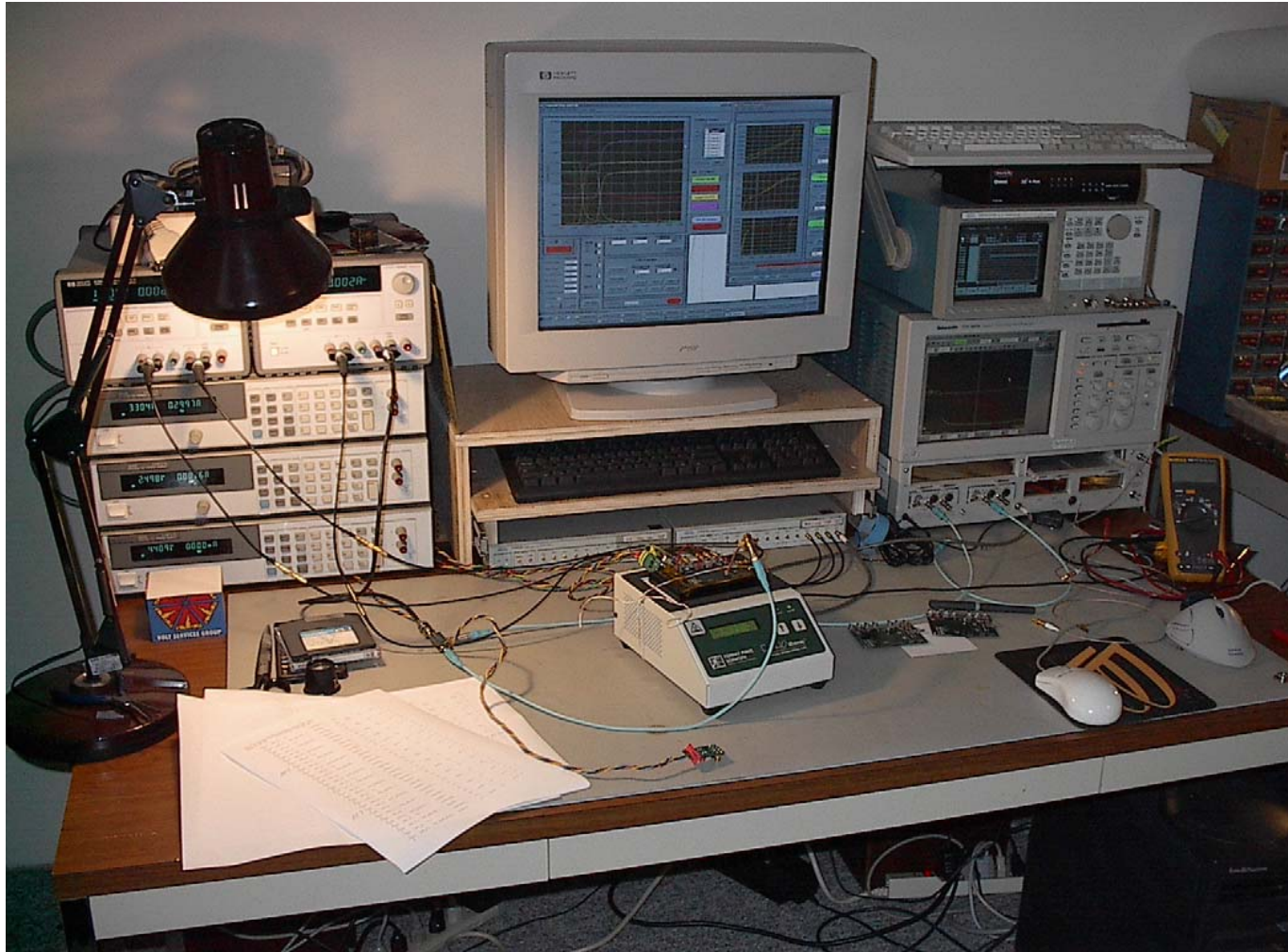
Industrial Infrastructure

- Free and commercial utilities
 - winibis, ibis2spice, ibisinf
 - Commercial viewers and development tools
- Internal company model development
 - Intel - IBIS Center
 - Siemens - Dogen
- IBIS model availability
 - 70+ semiconductor vendors - thousands of models
 - Teraspeed 13,500 models, 100+ vendors (next slides)

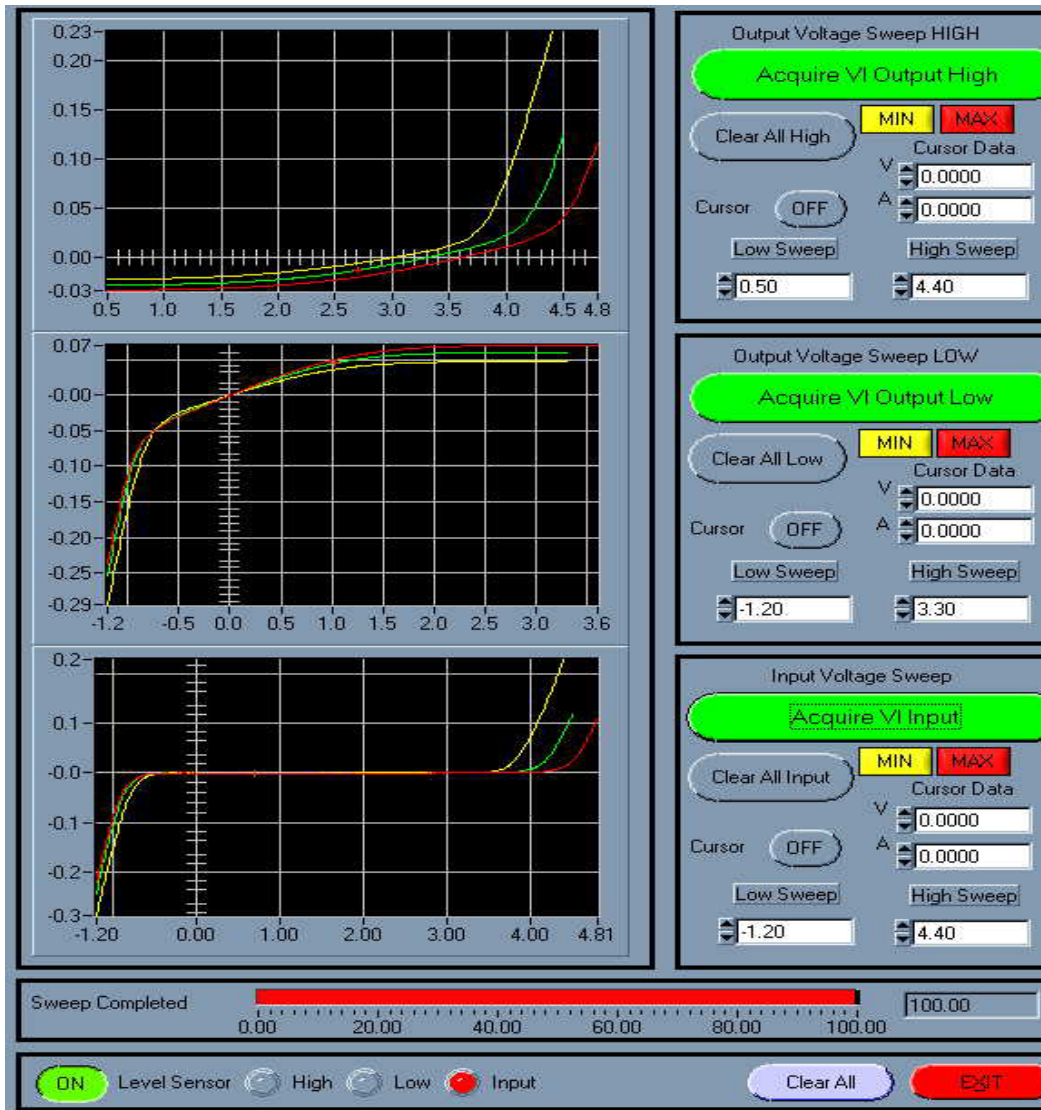


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Programmable Hardware and Fixturing

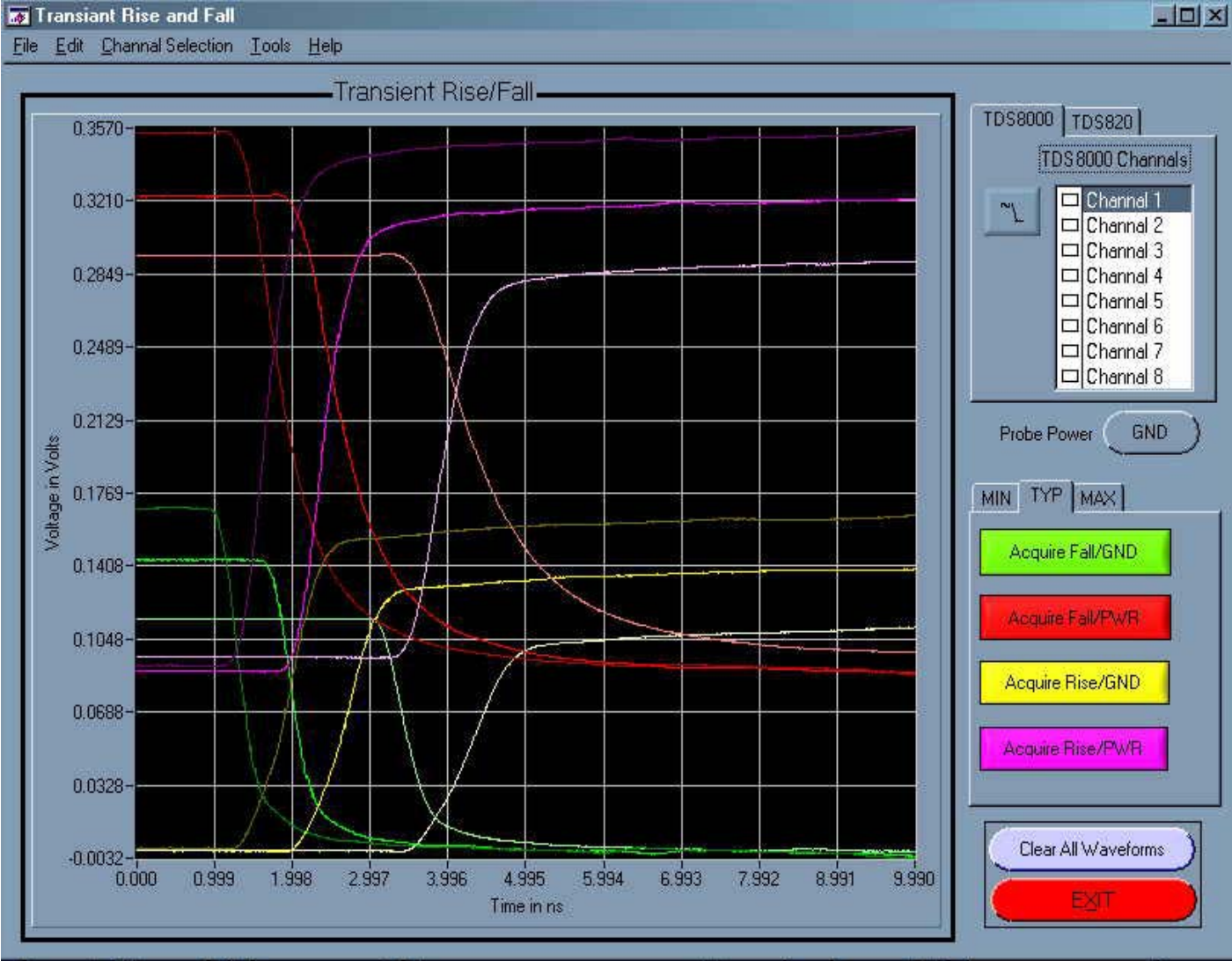


I-V Measurements (High, Low, High-Z or Input)



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Min-Typ-Max V-T Measurements



Database Management and Auto-generation of 13,500 IBIS Models

The screenshot displays the ZAP Model Builder 3.2 application window. The main window is titled "Restricted: Pins of part CY62147BV18LL-70" and contains a large table with columns: Part ID, Part ID, Name, Letter, Digit, Driver, Index, PWR, and GND. The table lists various pins such as 17934_BLE, 17934_DE, 17934_A0, etc., up to 17934_NC. Below the table are buttons for "Copy + Move Siblings", "Fill/Replace", and "Refresh".

On the right side, there is a "Devices by Part CY62147BV18LL-70" window showing a table with columns: Device ID, Part ID, Driver, Idx, Probe, Filename, Dcap, Param, Top, and tvm_r. It lists devices like 74609, 74611, and 74610.

Below the devices table is a "Quick Launch" window with input fields for Part ID (17934), Wild Part Name (*), Model ID, and Part Description, and a "Close" button.

At the bottom right, there is a "ZAP Model Builder 3.2" window with a "Zap" logo and buttons for "Parts", "Packages", "Libraries", "Tables", "Quick Launch", and "Exit Program".

The Windows taskbar at the bottom shows various open applications including Start, C:\models, 82546.ibs..., ZAPBuild3..., ZAP Mode..., Restricted..., Quick Lau..., Part Entrie..., Zeelan Ma..., Zeelan Ma..., Zeelan Ma..., Zeelan Ma..., Zeelan Ma..., 1:18 PM, N:\vint\82..., Adobe Acr..., Zeelan Ma..., Command..., IC_breaker, models.mdl, Microsoft..., All Library..., Library By..., modeler.b..., Pins of..., and Devices b...



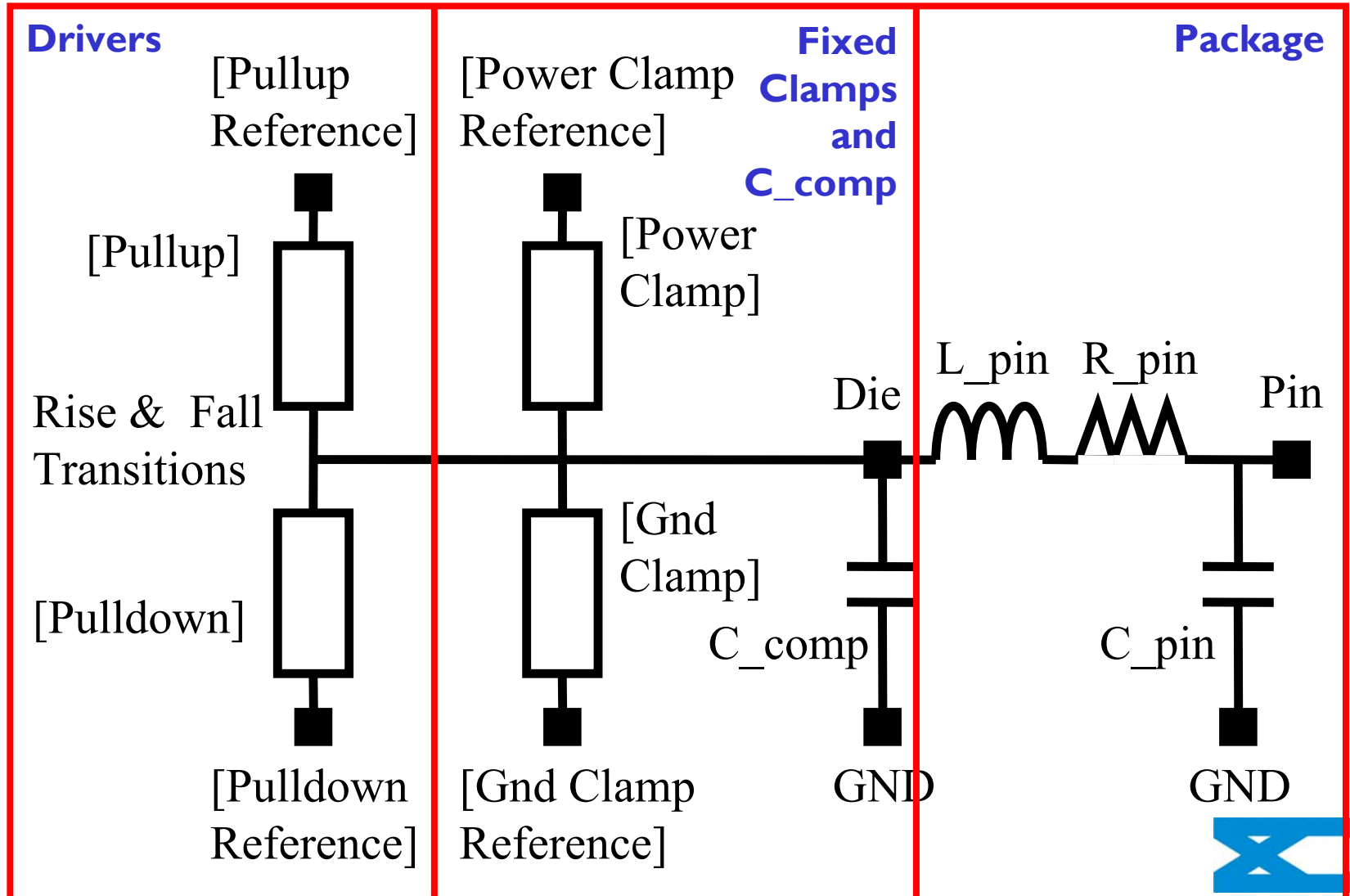
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IBIS Algorithms

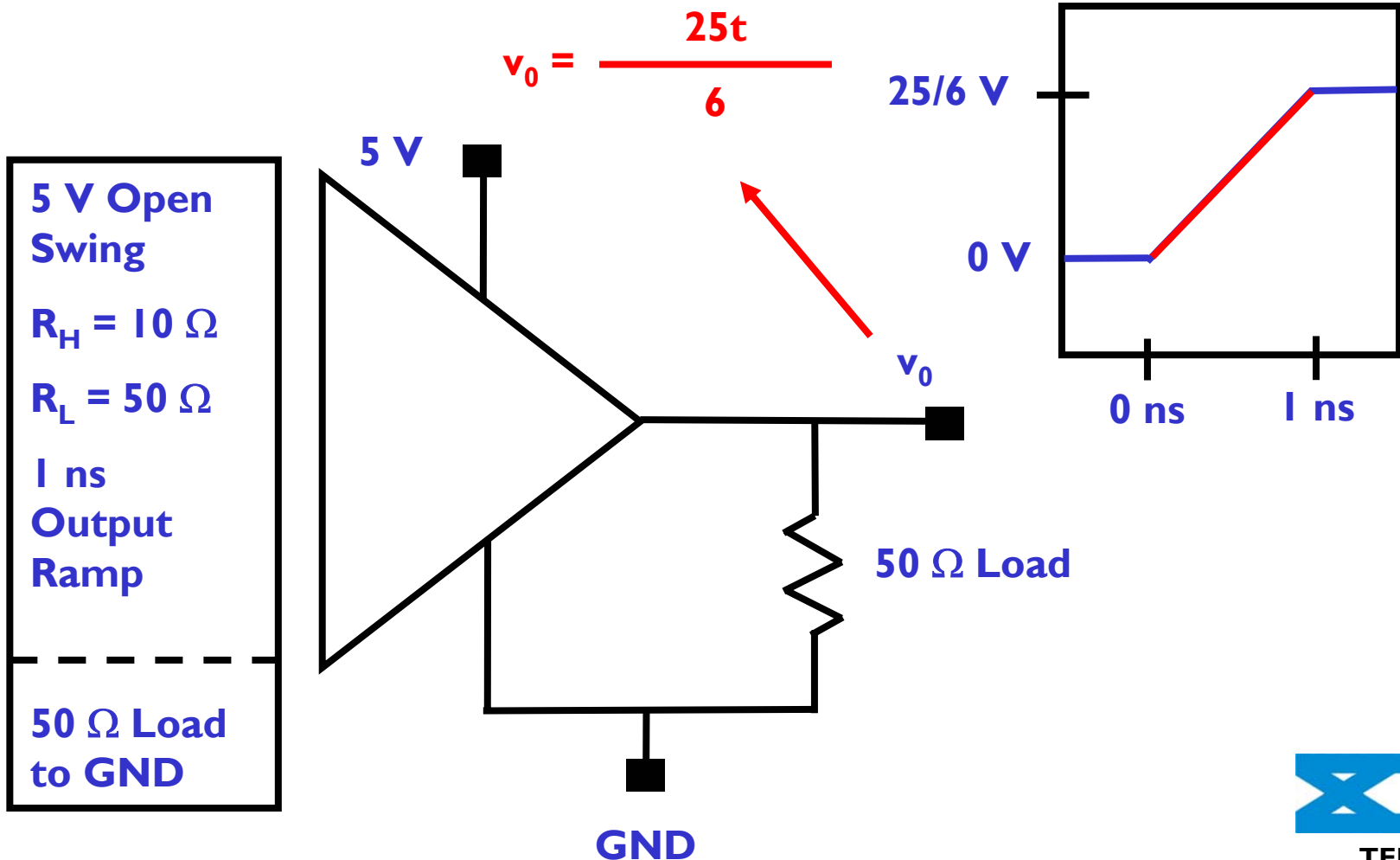
- IBIS data AND how processed
 - Older approaches give different solutions
 - Two-waveform algorithm gives good solutions
- Other algorithms
 - Multiple tables and dynamic interpolation
 - I/O Interface Model for Integrated Circuit (IMIC) for transistor multiple I-V and capacitance-V table interpolation
 - Radial based functions (RBF)



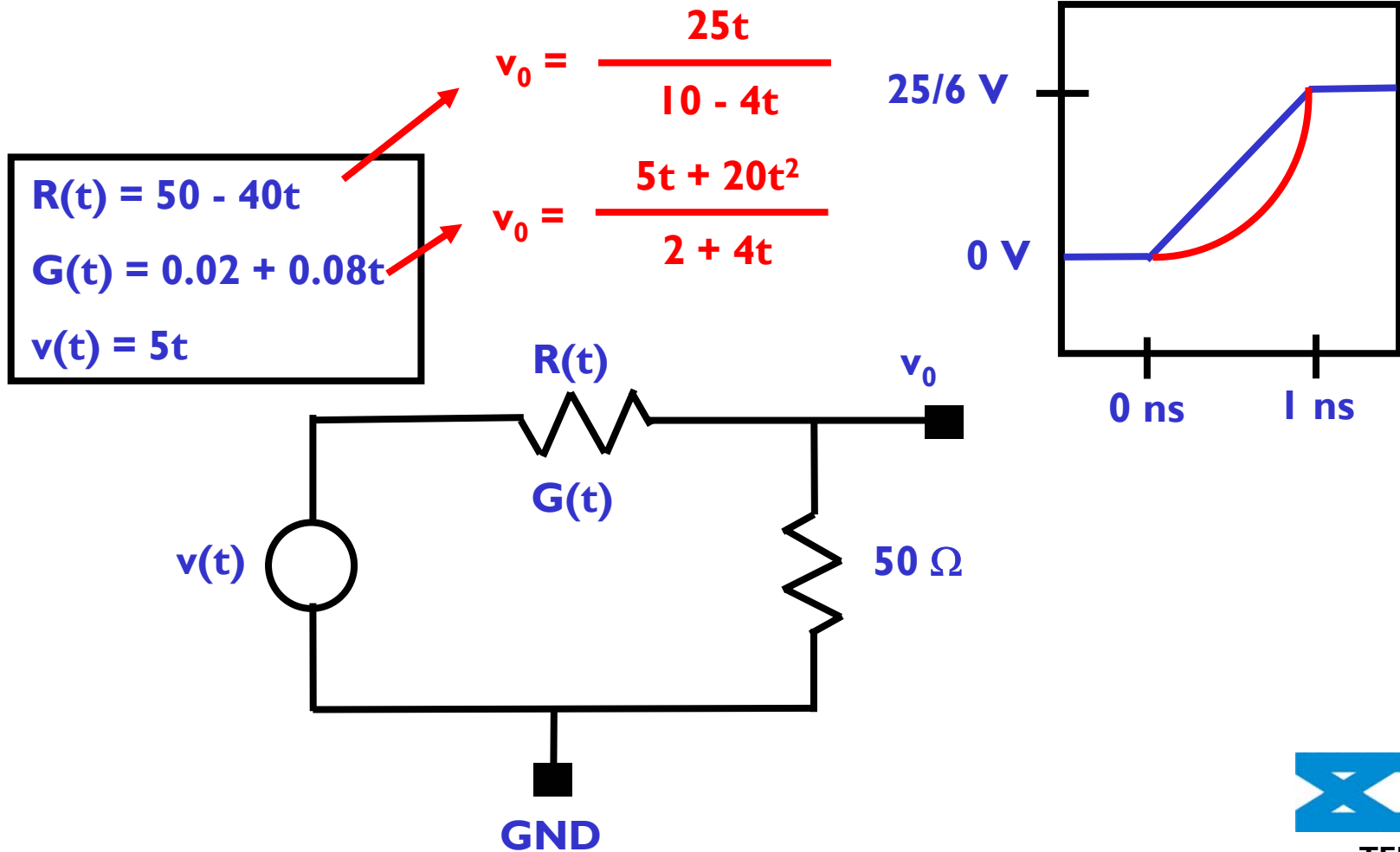
General IBIS Buffer Model



Example - Ideal CMOS Buffer



Thevenin Linear Z Transitions



Norton Linear Y Transitions

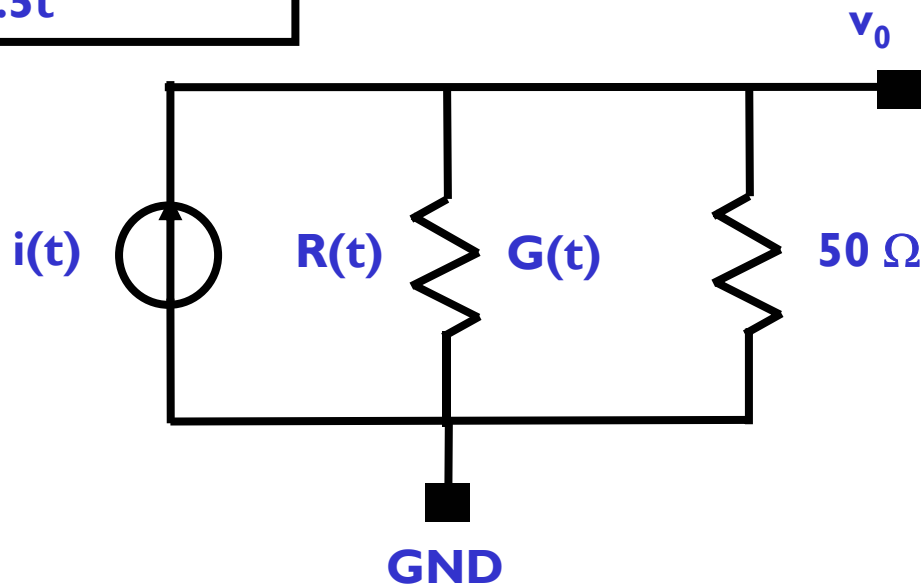
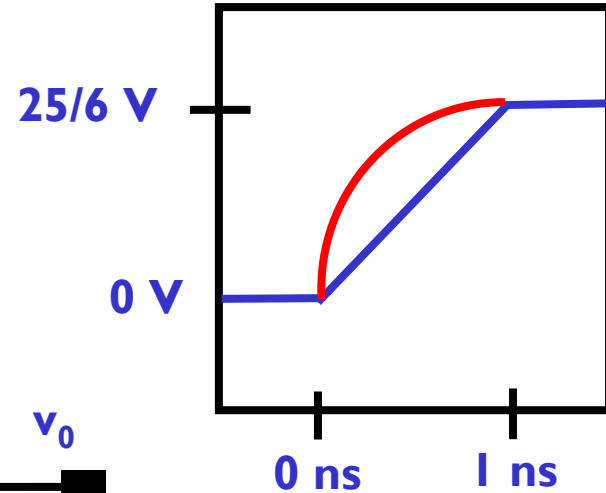
$$R(t) = 50 - 40t$$

$$G(t) = 0.02 + 0.08t$$

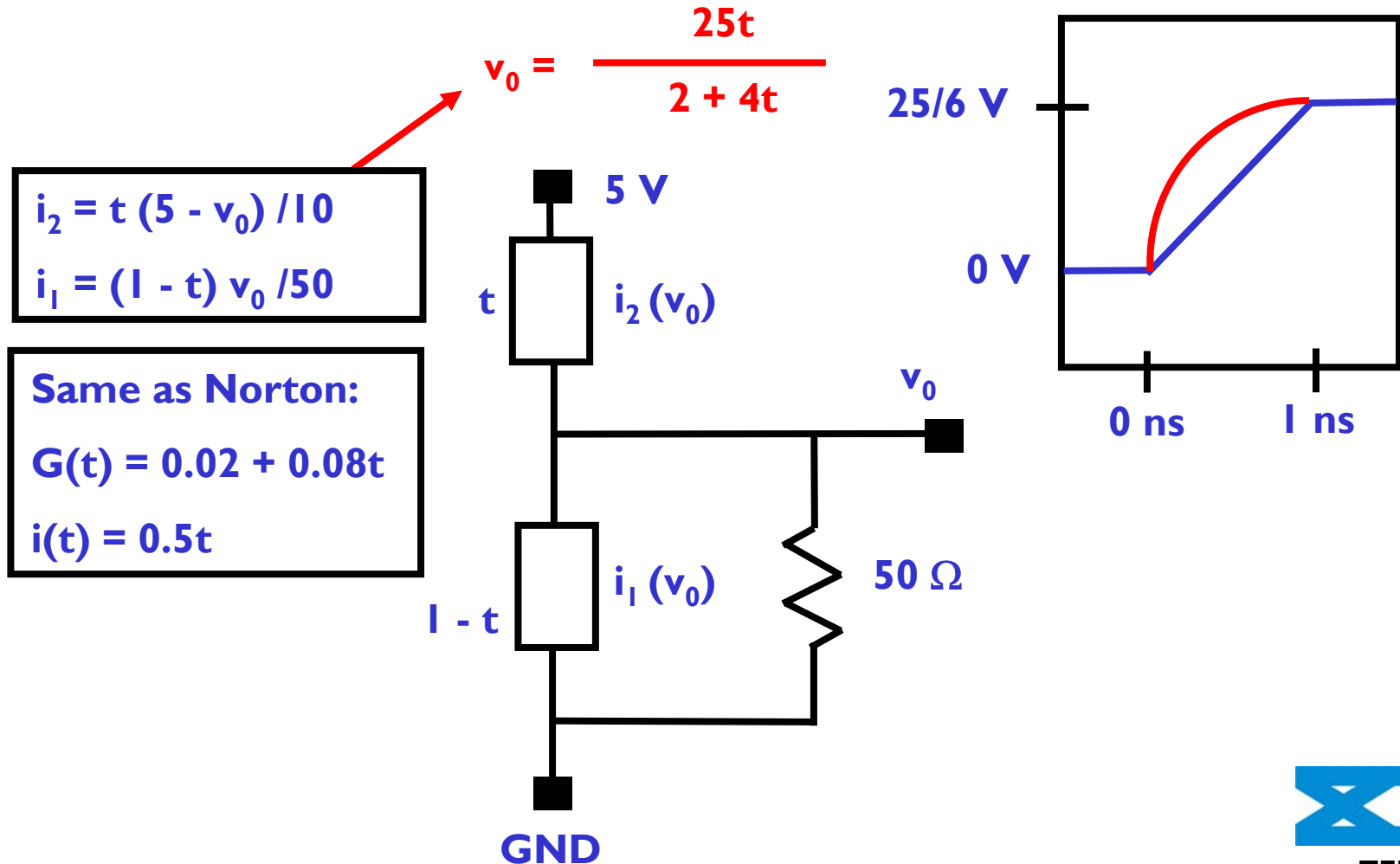
$$i(t) = 0.5t$$

$$v_0 = \frac{125t - 100t^2}{10 - 4t}$$

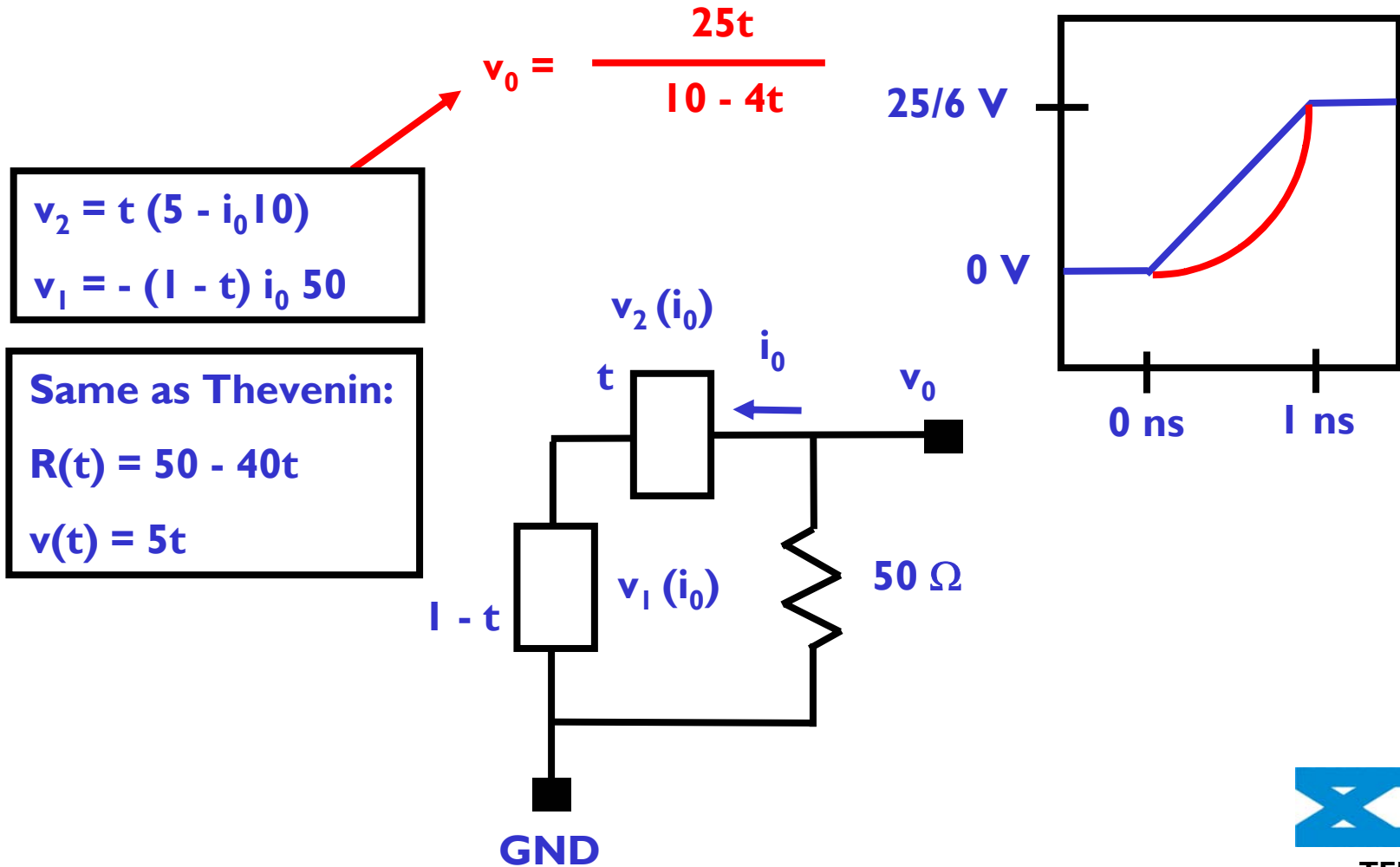
$$v_0 = \frac{25t}{2 + 4t}$$



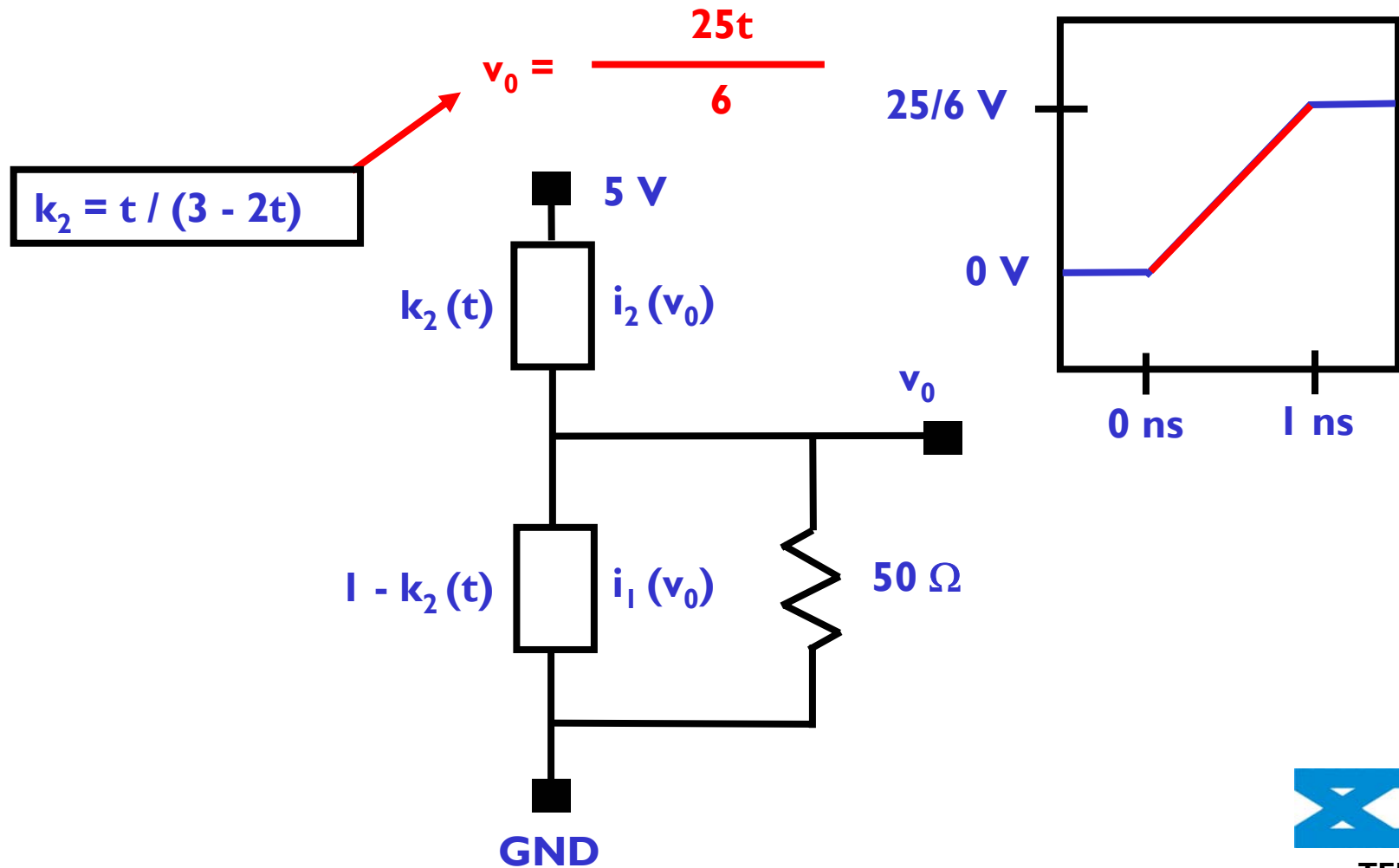
IBIS Linear Table Multipliers



Dual IBIS Linear Table Multipliers

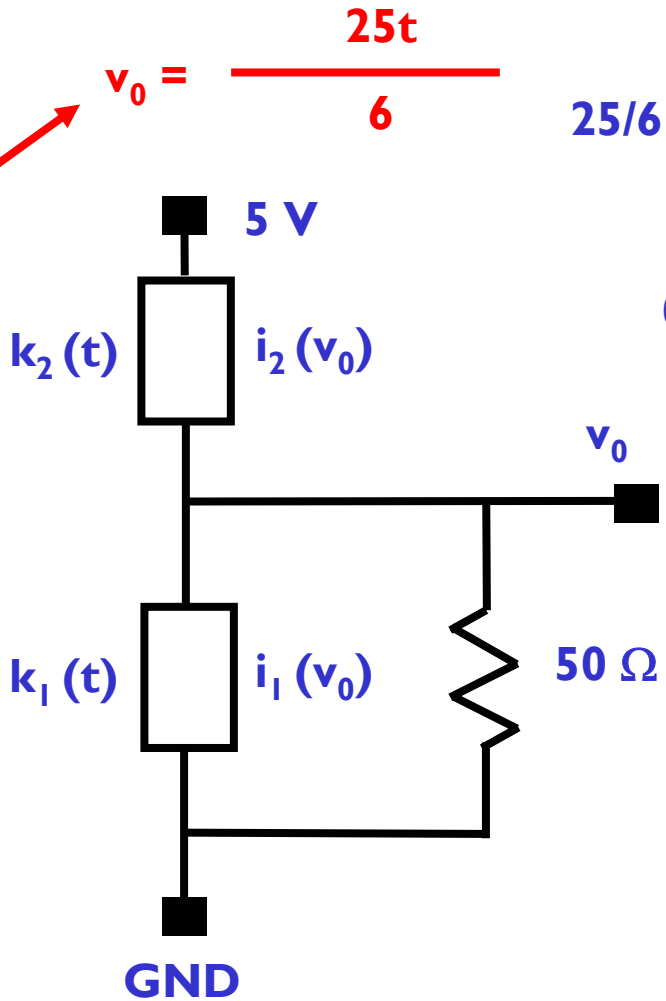


Dependent IBIS Table Multipliers

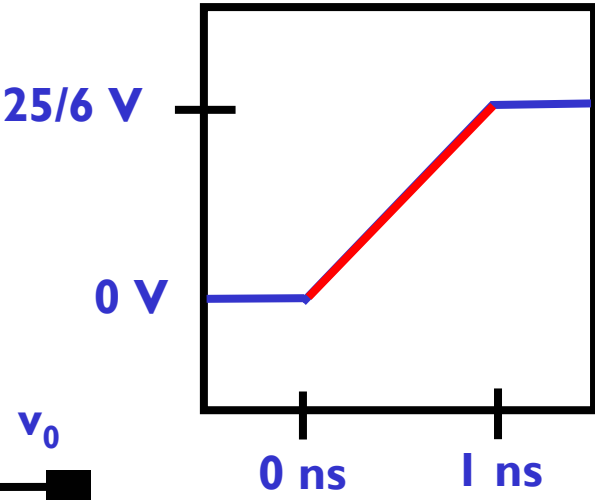


Independent IBIS Table Multipliers

k_2, k_1
 Independent from second waveform load and solution of two equations

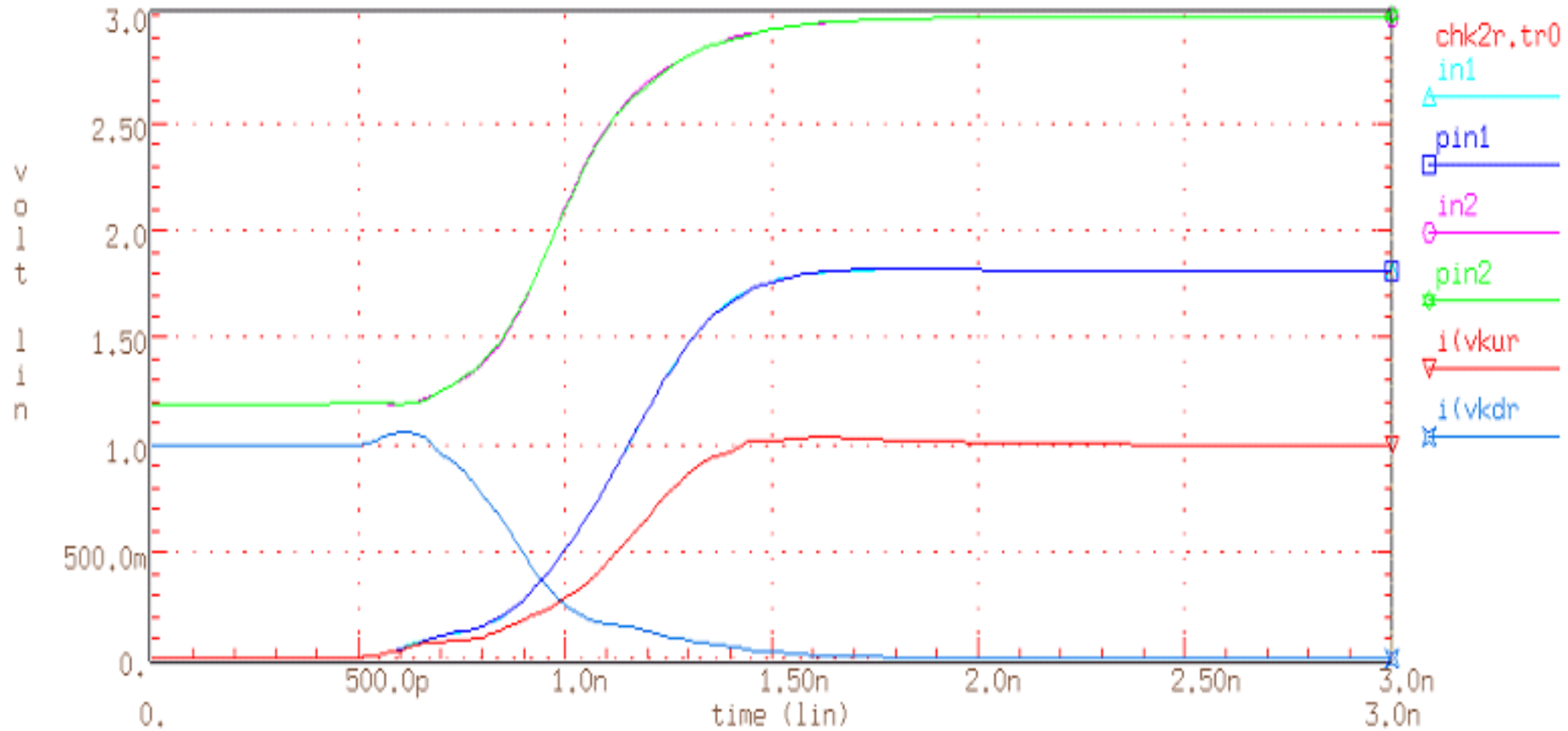


$$v_0 = \frac{25t}{6}$$

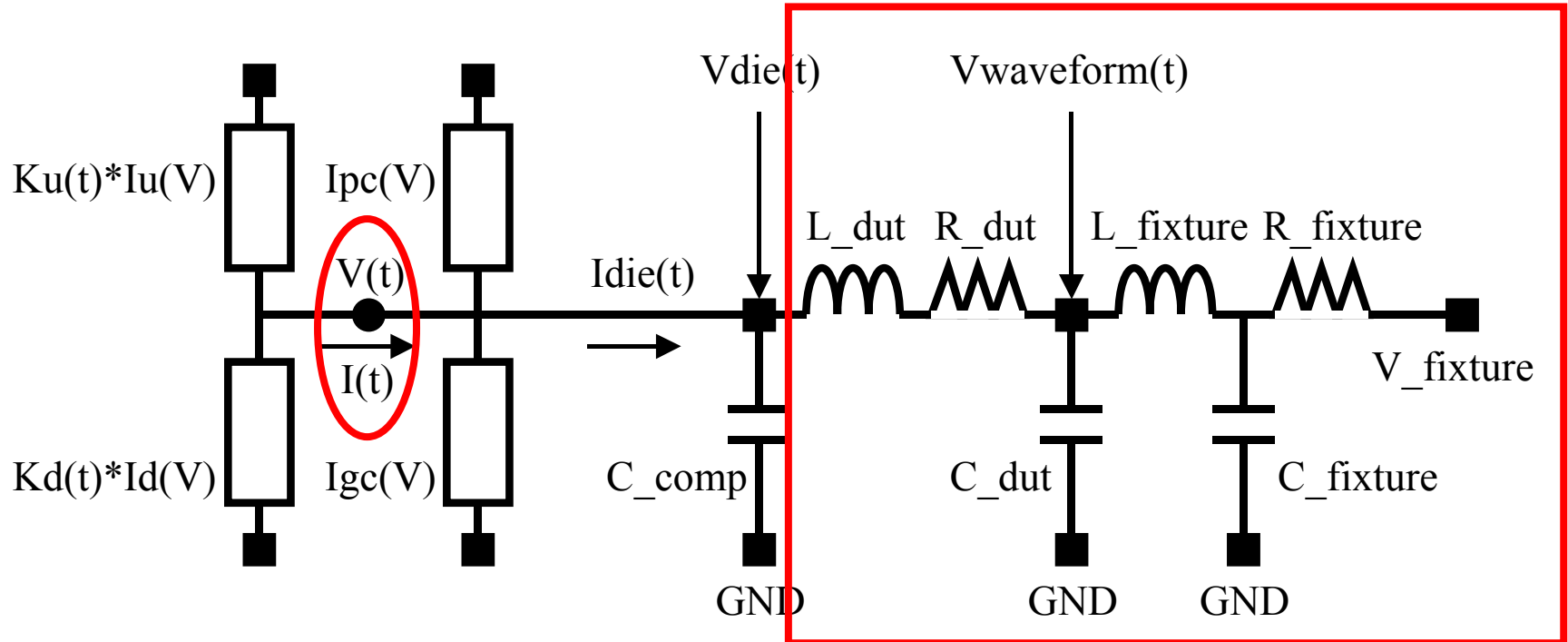


Actual Waveforms and Multipliers

* check 2 waveform rising calibration
98/10/09 06:53:21

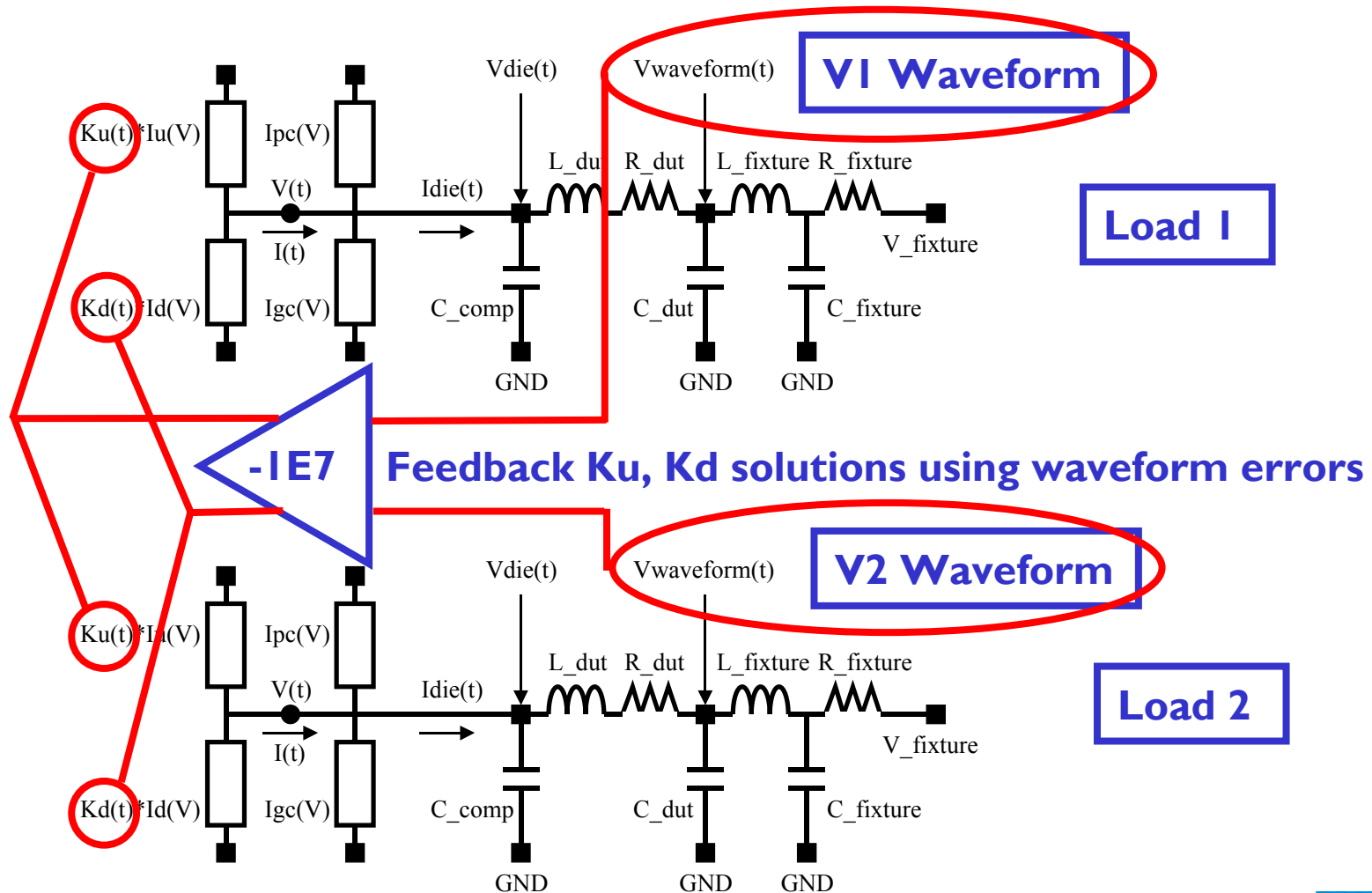


Generalized Test Load



$V(t)$ and $I(t)$ can be calculated from load information

SPICE Prototype for $K_u(t)$, $K_d(t)$



Feedback SPICE Circuit For Two Non-linear/Table Equations

```

*
* FEEDBACK TABLE ADJUSTMENT ..... VVV
GDET  NDET  GND  CUR=' ( I (VDN2) *I (VUP1) -I (VDN1) *I (VUP2) ) / ((1E7)) '
VDET  NDET  GND  0
*
GKUR   NKU   GND
+ CUR=' ( (V(IN2) -V(PIN2)) *I (VDN1) - (V(IN1) -V(PIN1)) *I (VDN2) ) /I (VDET) '
VKUR   NKU   GND  0
*
GKDR   NKD   GND
+ CUR=' ( (V(IN1) -V(PIN1)) *I (VUP2) - (V(IN2) -V(PIN2)) *I (VUP1) ) /I (VDET) '
VKDR   NKD   GND  0
*

```

Kur

Kdr

- $V1(t)/Z(t) = Ku(t)*Iu(V1(t)) + Kd(t)*Id(V1(t))$
- $V2(t)/Z(t) = Ku(t)*Iu(V2(t)) + Kd(t)*Id(V2(t))$



Part of SPICE Encoded IBIS Prototype

```

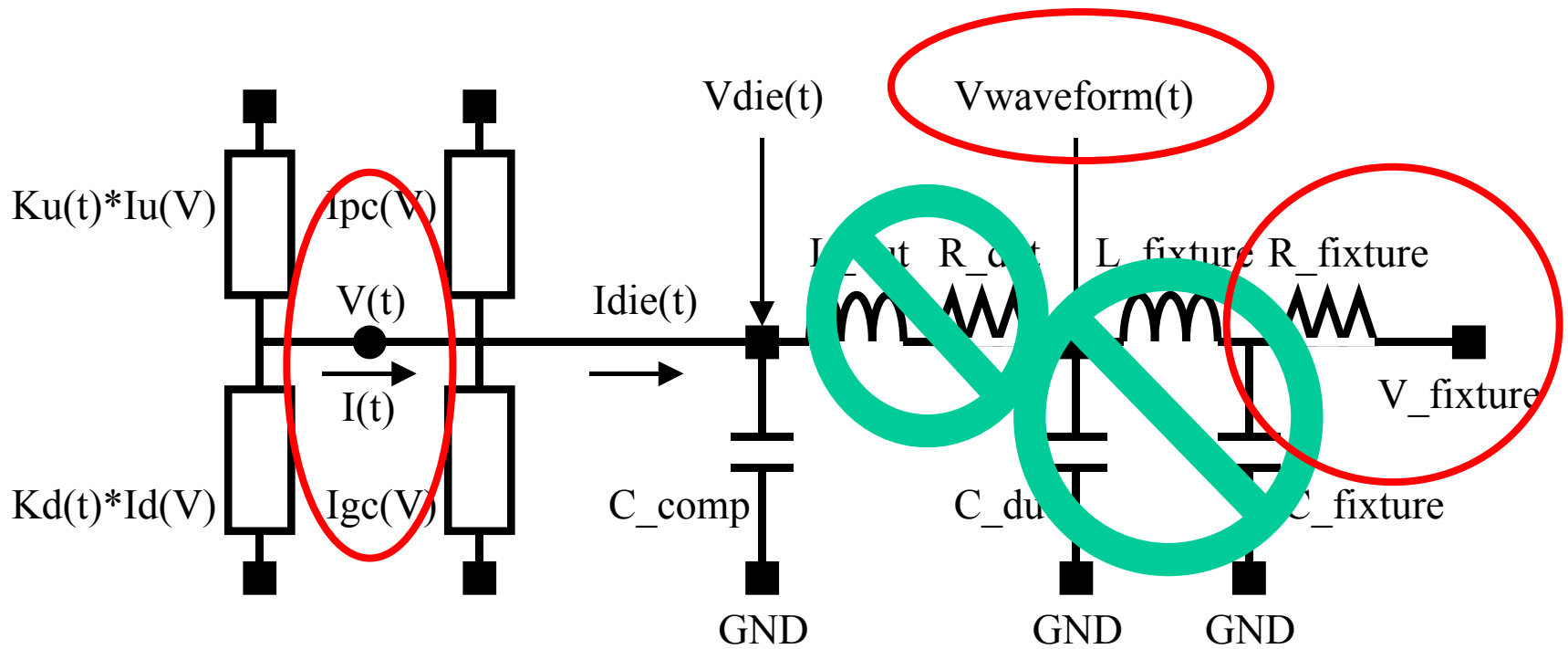
* HIGH SIDE
XUP  OUT1  VCC  NU1          PULLUP
VUP  NU1   VCC  0
GUP  OUT1  VCC  CUR=' -I (VUP) * ( I (VKUR) * I (VON) + I (VKUF) * (1-I (VON)) ) '
XPC  OUT1  VCC          POWER_CLAMP
*
* LOW SIDE
XDN  OUT1  GRD  ND1          PULLDOWN
VDN  ND1   GRD  0
GDN  OUT1  GRD  CUR=' -I (VDN) * ( I (VKDR) * I (VON) + I (VKDF) * (1-I (VON)) ) '
XGC  OUT1  GNDC  GND_CLAMP
*
* C_COMP AND DUT PACKAGE
XCAP  OUT1  GRD          C_COMP
XPKG  OUT1  GRD  PIN1      PACKAGE
*
* LOAD
TLOAD  PIN1  GRD  PIN9  GRD  Z0=50 TD=1N
RLOAD  PIN9  GND  50G
*
* VOLTAGE CONTROL (AMPLITUDE (0 TO 1), PULSE WIDTH & PERIOD)
VPULSE STEP  GRD  0  PULSE (1 0 0P 1P 1P 5N 10N)

```

Kur, Kdr

Kuf, Kdf

Recommended Test Load, Industrial usage



Recommended Loads:

50 Ω to V_{cc}

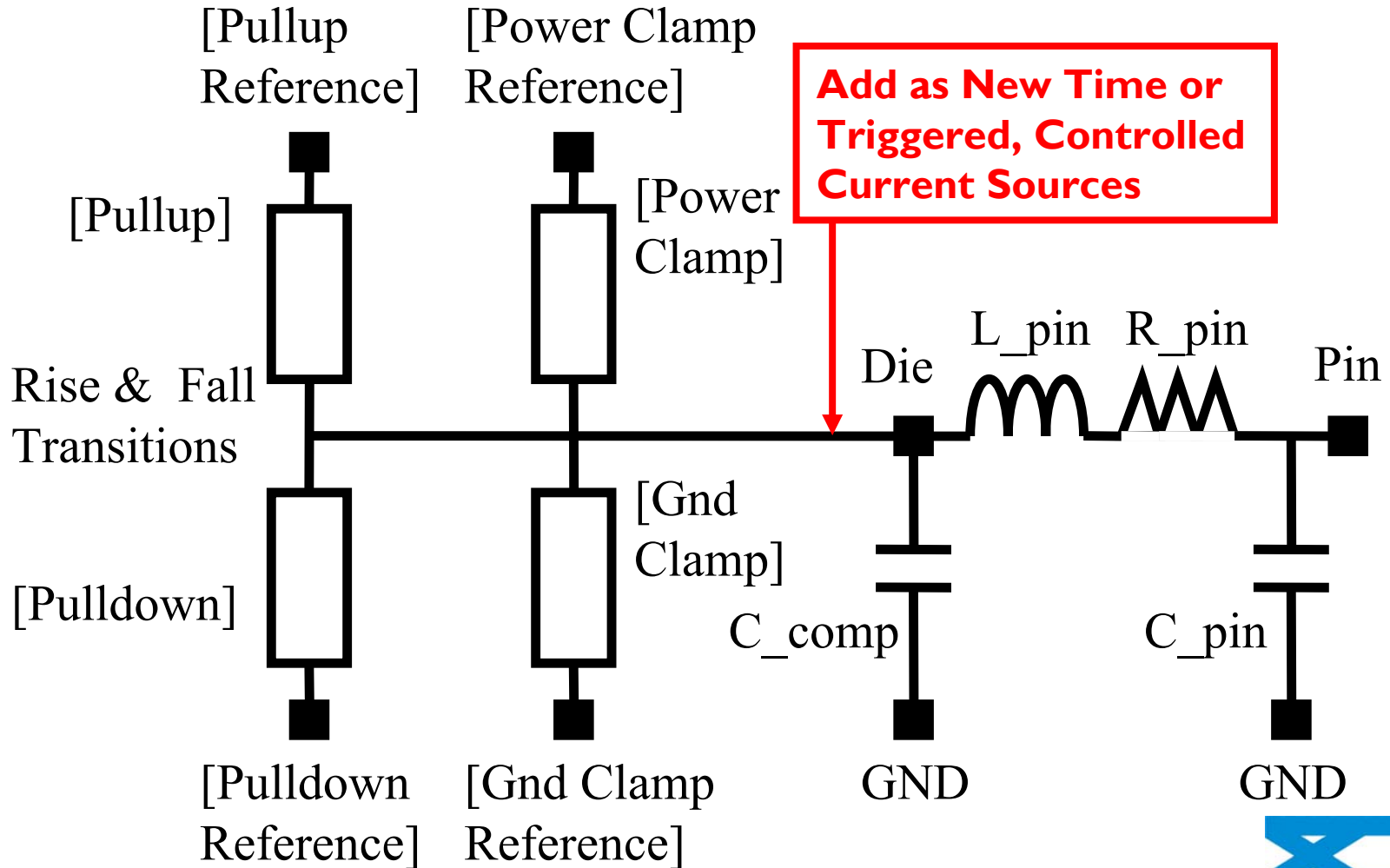
50 Ω to Gnd

IBIS Version 3.2/4.0 Additions

- Time controlled pre/de-emphasis (kickers) and multi-staged buffers [Driver Schedule]
- Submodels
 - Dynamic clamps
 - Bus hold
 - Triggered, switchable and modal terminators
 - Fall back (impedance controlled buffers)
- Other additions



Additions to IBIS Reference Model

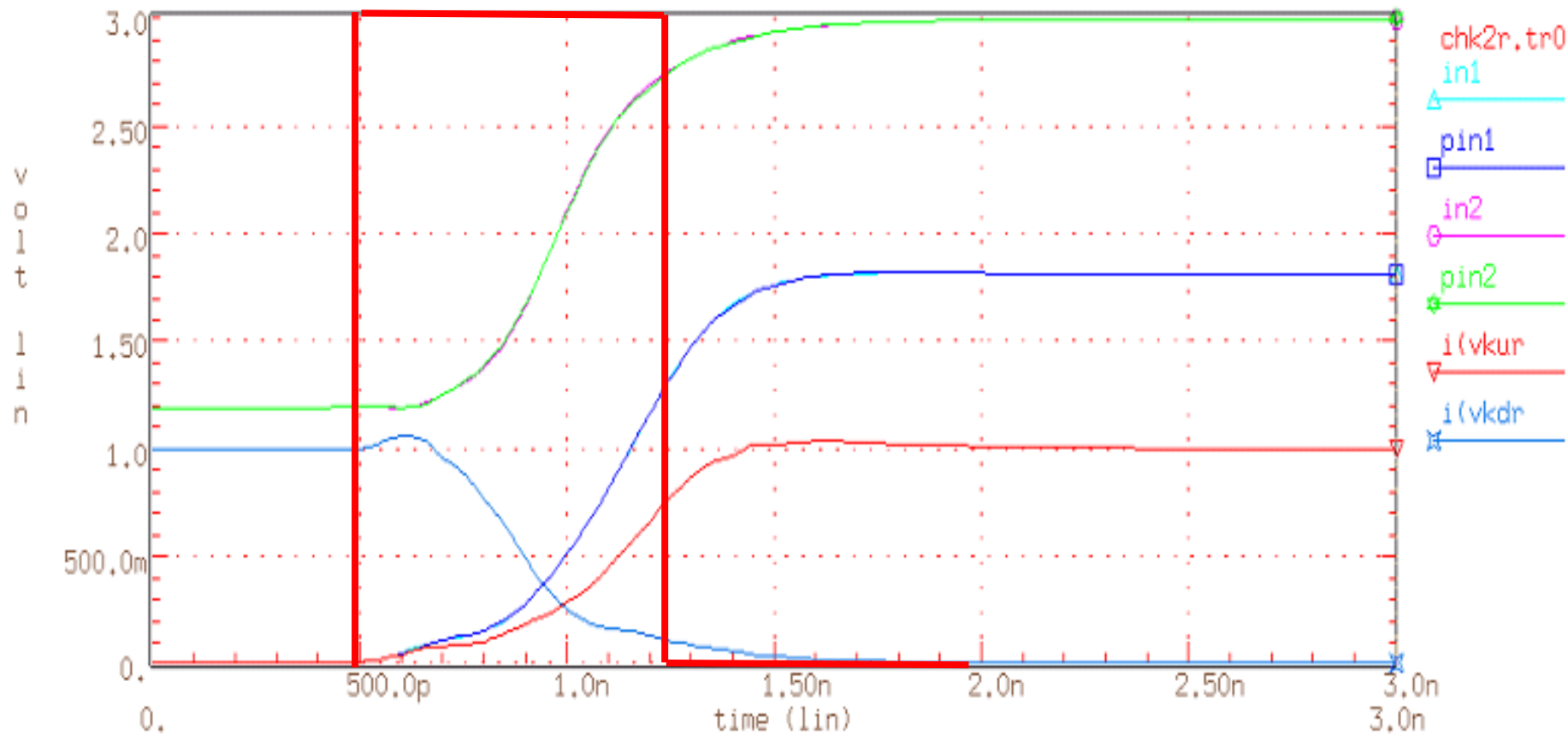


Problems and Limitations

- Ground, power currents a function of the model, may not be accurate
 - Gate modulation effects
 - Could be fixed with more tables or parameters
- Timing to internal buffer nodes
- Frequency dependent impedance models
- Delay timing errors with over-clocking - shown next

Over-clocking Problem with IBIS, No Simple Solution for Delays

* check 2 waveform rising calibration
98/10/09 06:53:21



Version 4.1 Multi-Lingual Addition

- Overcomes fixed format technical, process limits
- Complex buffer architectures handled through compiled/executable code
- On-die interconnect SPICE descriptions
- VHDL-AMS & Verilog-AMS logic control
- Opportunity for new features and approaches
 - ICEM buffer additions
 - RBF buffers and other code based models
 - Direct SPICE implementations

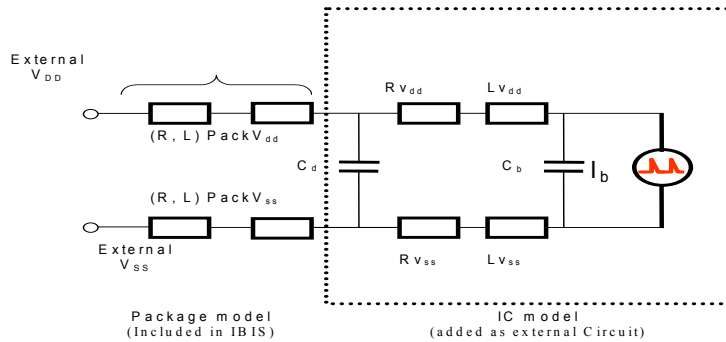


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ICEM External Circuit Supply Additions for Core Noise Modeling

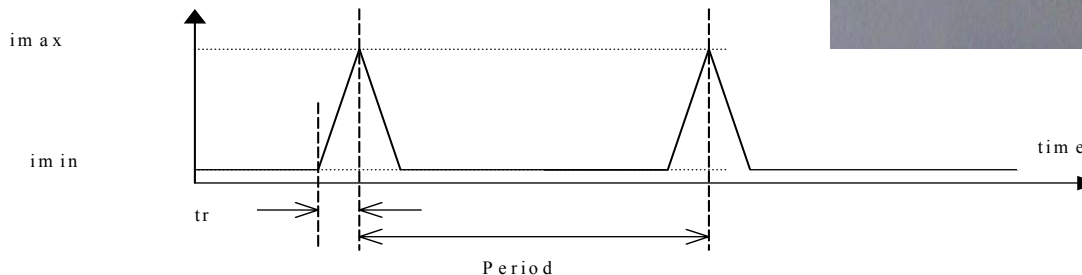
68HC12D60

ICEM MODEL



$L \text{ Pack}V_{SS} = 2.2 \text{ nH}$
 $L \text{ Pack}V_{DD} = 2.2 \text{ nH}$
 $C_d = 3.2 \text{ nF}$
 $R_{V_{SS}} = 2$
 $R_{V_{DD}} = 2$
 $C_b = 50 \text{ pF}$

Current generator I_b



Period = 31.25 ns.
 $I_{min} = 0.01 \text{ A}$
 $I_{max} = 0.4 \text{ A}$
 $T_r = 1 \text{ ns}$

SPICE model called by
[External Circuit]



Radial Based Function Model

- Gaussian base vectors
- [External Model] can be used for calling SPICE or other languages
- Similar to IBIS:
 - High state and low state set of bases
 - Input mode
- Independent of evolving structural details

Current Industrial Concerns

- Technical
 - Internally terminated differential buffers
 - Pre-emphasis needed for lossy lines
 - Higher-speed and over-clocked operation
 - Timing to internal locations
 - On die interconnect
 - Package and interconnect limitations
- Encryption and availability



Interconnect Specification

- Cascaded, coupled, uncoupled stages
 - RLGC form
 - Touchstone S-parameter format for losses
 - Reference document is uploaded on IBIS site
 - Time domain support excellent
- Swathing (expansion of middle region) since only a portion of connections are extracted

Conclusions

- IBIS well-known, accepted, widely used
- Well constructed IBIS models and good algorithms yield accurate results
- Practical extensions for complex buffers
- Multi-lingual format for executable extensions
- Interconnect structures are of interest